"Vega 10" Databook

Technical Reference Manual - AMD Confidential

Part Number: 56006_1.00

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Revision History

Note: The release states are defined as:

Preliminary Releases:

Revision numbers 0.xx are rough works.

Revision numbers 1.xx are documents with substantial info

Revision numbers 2.xx are documents with complete information.

Full Release

Revision numbers 3.xx are for production.

Revision History

Rev 1.00 (May 17, 2017)

- Preliminary release.

Contents

Figures

Chapter 1 Introduction

Chapter 2 Functional Overview

Chapter 4 Timing Specifications

Chapter 5 Electrical Characteristics

Chapter 7 Mechanical Data

Chapter 8 Boundary Scan Specification

Tables

Chapter 1 Introduction

Chapter 2 Functional Overview

Chapter 3 Signal Descriptions

Chapter 4 Timing Specifications

Chapter 5 Electrical Characteristics

Chapter 6 Thermal Data

Chapter 7 Mechanical Data

Chapter 8 Boundary Scan Specification

Appendix A Pin Listings

1 Introduction

TBD.

The features and functionalities identified in this databook are preliminary information and do not constitute specifications until they have been qualified by AMD.
The databook is updated as necessary following qualification to convert this document to a formal specification.

Please review any errata and advisories as they identify amendments to the specifications in this databook.

Contact your local AMD support person for the software support schedules of GPU features.

1.1 Part Identification

1.1.1 Packaging Types and Device IDs

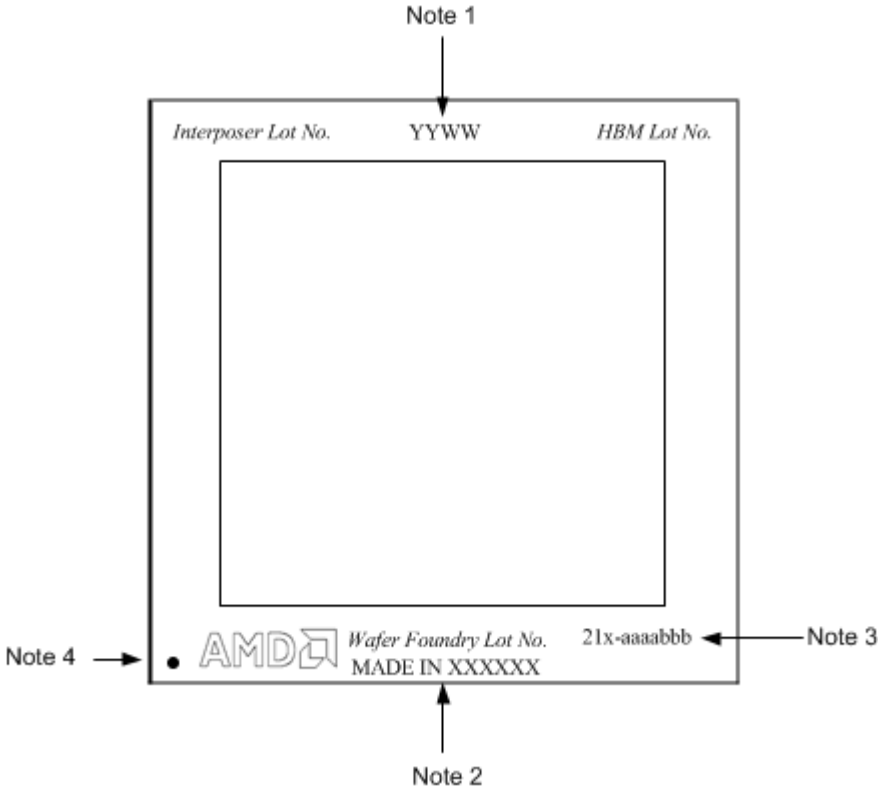
The vendor ID is 0×1002.

Table 1–1 Package Information

Part	Device ID / Revision ID	Part Number	HD Audio Controller ID	HD Audio Codec ID	Package
"Vega 10 - XTX"	6863/00	215-0894252	AAF8	AA01	2013 HFCBGA

1.1.2 Branding Format

Figure 1–1 "Vega 10" Branding



Note:

1. The date code where YY is the assembly start year and WW is the assembly start week. For engineering samples, ES is found after the date code.
2. Country of origin XXXXXX (The assembly site; such as USA, SINGAPORE, TAIWAN, and CHINA).
3. The part number. (Refer to Table 1–1 (p. 1).)
4. GPU Pin 1 Dot.

The branding format can be in laser, ink, or mixed laser and ink marking.

2

Functional Overview

This section describes the major subsystems and interfaces of "Vega 10". To go to a topic of interest, use the following list of linked cross-references:

2.1 Memory Interface

2.1.1 Memory Configurations Support

"Vega 10" adopts second generation HBM (high-bandwidth memory) technology with two HBM memory stacks embedded together with the GPU die through a silicon interposer. Therefore "Vega 10" designs do not need nor do they support external video memory.

Each memory stack has 16 pseudo channels of 64-bit width each. Therefore, the total interface between the GPU and memory is 2048-bits wide.

Table 2–1 HBM Configurations

Pseudo Channel Density in Gbit	Pseudo Channel Configuration Row x Col x Bank Address Bits	Pseudo Channel Width (bits)	Burst Length	Stack Size (16 Pseudo Channels) in GB	Total Frame Buffer Size (2 Stacks) in GB
4	14 x 5 x 5	64	4	8	16

2.1.2 Memory Aperture Size

The memory-aperture size can be set up through either pin straps for designs that do not have dedicated ROM for the video BIOS, or ROM straps for designs that have dedicated ROM. Refer to the descriptions of the ROM_CONFIG[2:0] and MEM_AP_SIZE [2:0] straps in Pin-based Straps (p. 37) for more information.

"Vega 10" requires dedicated ROM for video BIOS. Therefore, memory aperture size is set by ROM straps.

The memory aperture defines the address range that the CPU can access. The memory-aperture size assigned to the GPU by the system BIOS is different from the physical-memory size that the AMD display driver reports to the operating system and control panel. It does not limit the GPU's ability to use the entire frame-buffer memory at any time. Modern graphics and multimedia applications use drivers to alter the frame-buffer contents—direct manipulation of the frame buffer by the CPU is limited. Therefore, having a memory-aperture size that is smaller than the physical frame-buffer size does not limit performance. The AMD display driver reports the memory size based on the amount of physical VRAM installed on the card rather than the memory-aperture size.

Due to memory-management constraints, the memory-aperture size should be the same as the frame-buffer size for 64 MB, 128 MB, and 256 MB. For frame-buffer sizes larger than 256 MB, the memory-aperture size should be 256 MB. For designs requiring larger than 256 MB aperture size, consult with AMD.

2.2 Acceleration Features

- Support for DirectX® 12 (Feature Level 12_0) features, including the full-speed 32-bit floating point per component operation:
  - Shader Model 5.0 geometry and pixel support in a unified shader architecture:
    - Vertex, pixel, geometry, compute, domain, and hull shaders.
    - 32- and 64-bit floating-point processing per component.
    - New advanced shader instructions, including flexible flow control with CPU-level flexibility on branching.
    - A nearly unlimited shader-instruction store, using an advanced caching system.
    - An advanced shader design, with an ultra-threading sequencer for high-efficiency operations.
    - Graphics Core Next supporting native scalar instructions.
    - Advanced, high-performance branching support, including static and dynamic branching.
    - High dynamic-range rendering with floating-point blending, texture filtering, and anti-aliasing support.
    - 16- and 32-bit floating-point components for high dynamic-range computations.
    - Full anti-aliasing on renderable surfaces up to and including 128-bit floating-point formats.
    - A new read/write caching system, replacing texture cache with a unified read-write two-level cache.
- Support for OpenGL 4.5.
- Support for OpenCL™ 2.0.
- Support for Mantle
- Support for AMD LiquidVR™
- Anti-aliasing filtering:
  - 2×/4×/8× MSAA (multi-sample anti-aliasing) modes are supported.
  - A multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
  - Custom filter anti-aliasing with up to 12-samples per pixel.
  - An adaptive anti-aliasing mode.
  - Lossless color compression (up to 16:1).

- Anisotropic filtering:
  - Continuous anisotropic with 1× through 16× taps.
  - Up to 128-tap texture filtering.
  - Anisotropic biasing to allow trading quality for performance.
  - Improved anisotropic filtering with unified non-power of two-tap distribution and higher precision filter computations.
  - Advanced texture compression (3Dc+™).
  - High quality 4:1 compression for normal and luminance maps.
  - Angle-invariant algorithm for improved quality.
  - Single- or two-channel data format compatibility.
- 3D resources virtualized to a 40-bit virtual addressing space, for support of large numbers of render targets and textures.
- Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
- Programmable arbitration logic maximizes memory efficiency and is software upgradeable.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.
- Lossless z-buffer compression for both z and stencil.
- Fast z-buffer clear.
- Fast color-buffer clear.
- Z-cache optimized for real-time shadow rendering.
- Z- and color-compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

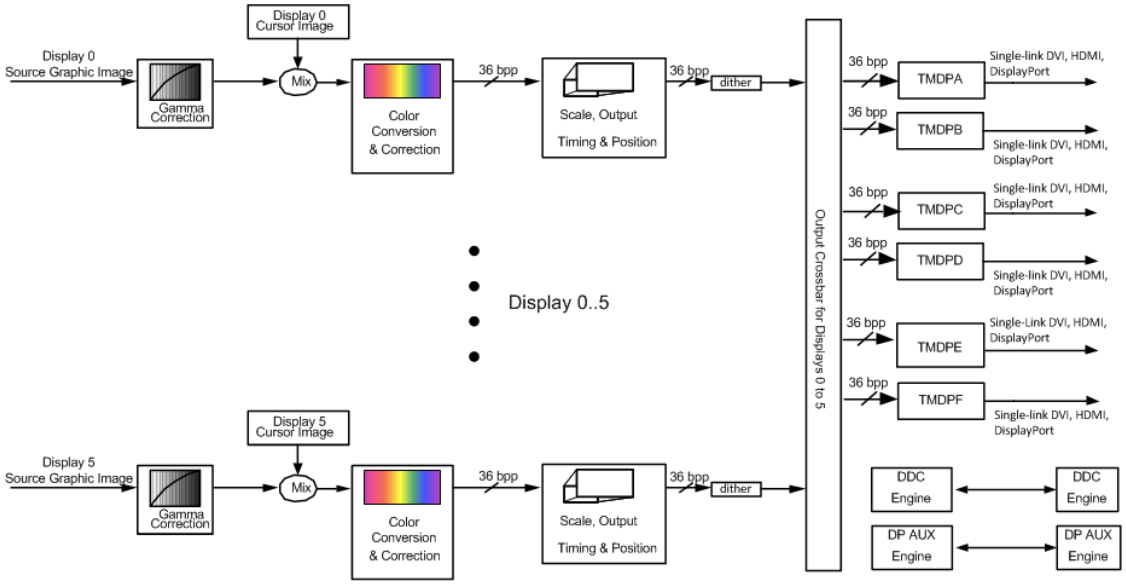
2.3 Display System

The display system supports accelerated display modes on up to six independent display controllers.

The full features of the display system are outlined in the following sections.

2.3.1 Display Features

Figure 2–1 "Vega 10" Display Top-level Data-flow Diagram



- Up to six independent display controllers that support up to true 36-bpp (bits per pixel) throughout the display pipe.
- Support for each display output type up to the following display timings:
  - DisplayPort 1.4 (HBR3):
    - Up to three 5120 × 2880 @ 60 Hz
    - Up to two 3840 × 2160 @ 120 Hz
    - Up to six 3840 × 2160 @ 60 Hz
    - One 7680 × 4320 @ 60 Hz using two DisplayPort cables
  - HDMI™ 2.0b (6 Gbit/s):
    - Up to six 3840 × 2160 @ 60 Hz or four 4096 × 2160 @ 60 Hz
  - Dual-link DVI:
    - Up to 2560 × 1600 @ 60 Hz or 1920 × 1200 @ 60 Hz
  - Single-link DVI:
    - Up to six 1920 × 1200 @ 60 Hz
- Advanced video capabilities, including high-fidelity gamma, color correction, and scaling for High Dynamic Range (HDR) or Standard Dynamic Range (SDR)
- A high-precision color pipe with the support of sRGB, Rec. 709 and Rec. 2020 color spaces with up to 12 bits/component
- HDR 10 support with HDMI 2.0b and DP 1.4 HDR scaling.
- Each display pipe includes a high-quality scaler for upscaling lower resolution desktop modes to available display resolutions or underscanning for the HDMI output (if needed):
  - All desktop sources up to 4096 pixels/line may be upscaled
  - Desktops up to 1920 wide may be underscanned for HDMI

- Support for Virtual Super Resolution (VSR) modes with surface sizes up to 5120 × 2880 downscaled to 3840 × 2160 @ 60 Hz
- HDCP supported independently and simultaneously on all HDMI, DVI, and DisplayPort outputs

  Note: HDCP is available only to licensed HDCP licensees and can only be enabled when connected to an HDCP-capable receiver.

  - Supports HDCP version 1.4/2.2 protection for the HDMI interface
  - Supports HDCP version 1.1/2.2 protection for the DisplayPort interface
  - Supports HDCP version 1.4 protection for the DVI interface
- Content adaptive LCD backlight modulation (VariBright) to reduce embedded display panel power consumption
- Support for Stereo 3D displays through HDMI, DisplayPort, eDP, and DVI. Includes frame-sequential and frame-packed full Stereo 3D modes. Also 2D frame-compatible modes including side-by-side, top-and-bottom, line interleaved, and pixel interleaved

2.3.2 DVI/HDMI™/DisplayPort/Embedded DisplayPort Features

- All TMDP links can be independently configured to any of single-link DVI, HDMI, DisplayPort (DP), or embedded DisplayPort. "Vega 10" also supports dual-link DVI. Contact AMD if the design requires native dual-link DVI support.
- See Table 3–5 (p. 23) for more information on the supported display interface combinations
- Optional dithering or frame modulation from the 36-bpp internal display pipeline to 24-bit or 30-bit outputs on DVI, HDMI, and DisplayPort if not using a 36-bpp output mode
  - Reduction to 18-bit is available for embedded DisplayPort outputs.

2.3.2.1 DVI/HDMI™ Features

- Supports industry-standard CTA-861 video modes including 480p, 720p, 1080i, 1080p, and 2160p. For a full list of currently supported modes, contact your local AMD support representative
- Supports AMD FreeSync™ technology on HDMI using AMD's vendor specific extension:
  - Fully HDMI compliant
  - Requires at least one display that is capable of AMD HDMI FreeSync™ technology
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—165 MP/s (megapixels per second) for single-link DVI
  - DVI—330 MP/s for dual-link DVI
  - HDMI—594 MP/s

Table 2–2 HDMI™ Features

HDMI Feature	Support
Link Capabilities	
Maximum Signal Bandwidth (MHz)	594*
Maximum HDMI Data Bandwidth (Gbit/s)	3 × 5.94 = 17.82
Video Capabilities	
Maximum 2D Resolution	1920 × 1080p @ 144 Hz, 36 bpp 2560 × 1440 @ 100 Hz, 30 bpp 2560 × 1440 @ 144 Hz, 24 bpp 3840 × 2160 @ 60 Hz, 24 bpp 4096 × 2160 @ 60 Hz, 24 bpp 3840 × 2160 @ 30 Hz, 36 bpp 4096 × 2160 @ 30 Hz, 36 bpp
RGB	Yes
YCbCr 4:4:4 / YCbCr 4:2:2 / YCbCr 4:2:0	Yes
xvYCC	Yes
HDMI Deep Color	Yes
HDMI 2.0b HDR	Yes
Maximum 4:4:4/4:2:2/4:2:0 Color Depth (bits per component)	12
PCM (Pulse-code Modulation) Audio Capabilities	
PCM Audio Rates Supported (kHz)	192, 96, 48, 176.4, 88.2, 44.1, 32
PCM Audio Bits per Sample	24, 20, 16
Maximum PCM Audio Channels	8
Maximum PCM Audio Bandwidth (rate × bits × channels) (Mbps)	36.864
Compressed-audio Capabilities	
Maximum Compressed-audio Bandwidth (Mbps)	24.576
Specific non-PCM Audio-format Support	
IEC 61937 Compressed-format support. For example, 5.1-channel Dolby DTS and 5.1-channel AC-3.	Yes
Dolby®-TrueHD Bitstream Capable	Yes
DTS-HD Master-audio Bitstream Capable	Yes
DVD-A (DST) Support	No
SACD (DSD) Support	No
Stereo 3D Display Capabilities	
Packed Frame Stereo 3D Video Formats	2160p @ 30/25/24 Hz, 1080p @ 120/100/60/50/30/25/24 Hz, 720p @ 120/100/60/50/30/25/24 Hz
Note: *** Applies to direct connections where GPU and HDMI connectors are on the same PCB with maximum trace lengths of 127 mm or 5 inches, otherwise re-driver is needed.**	

2.3.2.2 DisplayPort (DP) and Embedded DisplayPort (eDP) Features

- Supports all the mandatory features of the *DisplayPort Standard Version 1.4* and the following optional features on all links:
  - HBR3 (8.1 Gbps) support
  - HDR protocol support
  - ACM packet-type support
  - ISRC packet-type support
- DisplayPort Multi-streaming Transport (MST) allowing up to four display pipelines to drive a single DisplayPort interface (provided the DisplayPort link bandwidth is not exceeded)
- Supports AMD FreeSync™ technology, which dynamically synchronizes the refresh rate of a display with the frame rate of the GPU:
  - Based on DisplayPort Adaptive-Sync technology
  - Requires at least one display that is capable of DisplayPort Adaptive-Sync technology
- Each DisplayPort link can support three options for the number of lanes and four options for link-data rate as follows:
  - Four, two, or one lane(s)
  - 8.1*-, 5.4-, 2.7-, or 1.62-Gbps link-data rate per lane
  - The eDP mode port also supports the 4.32-, 3.24-, 2.43-, or 2.16-Gbps link rate option

Note: *Although GPU can support 8.1 Gbps link data rate, in eDP applications, GPU is validated up to 5.4 Gbps data rate due to unavailability of 8.1 Gbps capable TCONs.

- Supports RGB formats 24, 30, and 36 bpp, as well as 18 bpp RGB for eDP
- Supports YCbCr formats in 4:4:4, 4:2:2, and 4:2:0 and 8, 10, and 12 bits/component using Rec. 709 and Rec. 2020
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth
  - Example of supported pixel rate/resolution support for four lanes at 8.1-Gbps link rate:
    - 5120 × 2880 @ 60 Hz, 24 bpp is supported using VESA timings @ 938.25 MP/sec
    - 3840 × 2160 @ 120 Hz, 24 bpp is supported using VESA timings @ 1075.804 MP/sec
  - Examples of supported pixel-rate/resolution for four lanes at 5.4-Gbps link rate:
    - 3840 × 2160 @ 60 Hz, 24 bpp or 30 bpp is supported using VESA timings @ 533.25 MP/sec
    - 3840 × 2160 @ 60 Hz, 24 bpp or 30 bpp is supported using CTA timings @ 594 MP/sec
    - 4096 × 2160 @ 60 Hz, 24 bpp or 30 bpp is supported using CTA timings @ 594 MP/sec
    - 2560 × 1440 @ 144 Hz, 24 bpp is supported using CTA timings @ 586.586 MP/sec
  - Examples of supported pixel-rate/resolution for two lanes at 5.4-Gbps link rate:
    - 2560 × 1600 @ 60 Hz, 24 bpp or 30 bpp is supported using VESA timings @ 268.5 MP/sec
  - The following table shows the maximum pixel rates for four, two, or one lane(s) at 8.1-GHz link rate.

Table 2–3 Maximum Pixel Rates for 4, 2, or 1 Lane(s) at 8.1-GHz Link Rate

	18 bpp	24 bpp	30 bpp	36 bpp
One Lane	360 MP/s	270 MP/s	216 MP/s	180 MP/s
Two Lanes	720 MP/s	540 MP/s	432 MP/s	360 MP/s
Four Lanes	1080 MP/s	1080 MP/s	864 MP/s	720 MP/s

- Embedded DisplayPort (eDP) specific features:
  - Supports VESA eDP spec version 1.4
  - Supports protected content on eDP via ASSR and HDCP
  - Panel Self Refresh (PSR) support as per eDP 1.4 specification for optimal power reduction when in static screen condition
  - AMD FreeSync™ is used as a power-savings feature in eDP applications

2.3.3 Integrated HD-Audio Controller (Azalia) and Codec

- Each HDMI and DisplayPort output supports HD audio stream independently, up to a maximum of six output streams
- Maximum output bandwidth of 73.728 Mbit/s
- Low power ECN support
- Hardware silent stream for power optimization during no audio periods
- Function level reset
- Compatible Microsoft® UAA driver support for basic audio
- For advanced functionality (as follows), an AMD or a third party driver is required
- LPCM:
  - Speaker formats: 2.0, 2.1, 3.0, 4.0, 5.1, 6.1, and 7.1
  - Sample rates: 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
  - Bits per sample: 16, 20, and 24
- Non-HBR compressed audio pass-through up to 6.144 Mbps:
  - Supports AC-3, MPEG1, MP3 (MPEG1 layer 3), MPEG2, AAC, DTS, ATRAC, Dolby Digital+, WMA Pro, and DTS-HD
- HBR compressed audio pass-through up to 24.576 Mbps:
  - Supports DTS-HD Master Audio and Dolby True HD
- Plug-and-Play:
  - Sink audio format capabilities declaration
  - Sink information
  - AV association
- Lip sync information
- HDCP content protection
- DisplayPort supports Global TimeCode using the regular AUX channel—GTC master mode only

2.4 Video Acceleration Features

UVD video decoder acceleration technology:

- Dedicated Unified Video Decoder (UVD) for HEVC (H.265), H.264, VC-1/ WM9, MPEG-4 part 2, MPEG-2, and MVC decode:
  - HEVC Decode:
    - Implementation is based on the ITU-T H.265 v.1 specification
    - Supports Main/Main 10 profiles, Level 5.1
    - Supports up to 4096 × 2160 resolution at 60 fps
    - Up to a bit rate of 160 Mbps
    - Supports HDR-10 video playback
  - H.264 Decode:
    - Implementation is based on the ISO/IEC 14496-10 specification
    - Supports up to High profile, Level 5.2—Support for Constrained Baseline profile (no FMO, no ASO) only
    - Supports up to 4096 × 2160 resolution at 60 fps
    - Up to a bit rate of 160 Mbps
    - Supports MVC decode for Blu-ray 3D content
    - Supports up to 18 HD streams (1080p) at 30 fps each
  - VC-1 Decode:
    - Implementation based on the SMPTE 421M specification
    - Supports up to AP @ L3
    - Supports up to 1080p @ 60 fps
    - Maximum bit rate of 40 Mbps
  - MPEG-4 Part 2 Decode:
    - Supports up to ASP @ L5, high-definition profiles
    - Sprite, GMC (global motion compensation), and RVLC (reversible variable length coding) are not supported
  - MPEG-2 Decode:
    - Implementation based on the ISO 13818-2 specification
    - Supports up to MP @ HL
  - MJPEG Decode:
    - Implementation is based on the ISO/IEC 10918-1 specification
    - Supports Baseline (DCT based, interleaved only)
    - Supports up to 8K × 8K resolution (TBD)
    - JFIF input format

        - 4:2:0 and 4:2:2 format support
        - Reference performance: 1080p @ 60 fps (TBD)
        - MJPEG decoder can operate concurrently with other video decode or encode operations
    - Supports premium content DRM.
    - Microsoft DirectX video acceleration (DXVA) application programming interface (API) for Windows® operating systems (both DX9 and DX11.1 variants).

UVD Video Encoding acceleration technology:

- HEVC Encode:
    - Encode is frame interleaved with video decoder
    - Based on the ISO/IEC 23008-2 specification.
    - Maximum resolution supported is 4096 × 2176
    - Constant bit rate and variable bit rate rate controls
    - Supports SR-IOV virtualization

Video processing acceleration:

- Implemented using GCN shaders for compute.
- Video scaling and YCrCb to RGB, RGB to YUV color-space conversion for video playback and fully-adjustable color controls.
- Motion-adaptive and vector-based deinterlacing filter eliminates video artifacts caused by displaying interlaced video on non-interlaced displays, analyzing the image, and using the optimal deinterlacing function on a per-pixel basis.
- Temporal and spatial noise removal, detail enhancement, color enhancement, cadence detection, sharpness, and advanced deinterlacing.
- Advanced upscaling of SD content to HD resolution.
- Multi-planes compositing engine for advanced video applications.

Supports top-quality DVD, Blu-ray, Netflix, and YouTube playback with the lowest CPU usage.

2.5 Video Codec Engine (VCE) Features

- Video encoding technology:
    - Video codec engine (VCE):
    - H.264 encoding is based on the ISO/IEC 14496-10 specification.
    - Maximum resolution supported is 4096 × 2176
    - H.264 Scalable Video Coding (SVC) temporal video encoding.
    - Constant bit rate and variable bit rate rate controls.
    - Supports SR-IOV virtualization

2.6 PCI Express® Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 3.0, up to 8.0 GT/s.
- Supports ×1, ×2, ×4, ×8, and ×16 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×16 lane reversal where the receivers on lanes 0 to 15 on the graphics endpoint are mapped to the transmitters on lanes 15 down to 0 on the root complex.
- Supports ×16 lane reversal where the transmitters on lanes 0 to 15 on the graphics endpoint are mapped to the receivers on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

2.7 Power Management Features

- Intelligent monitoring and control of power, current and temperature through AMD PowerTune technology:
  - Includes temperature monitoring and control of the GPU as well as HBM memory.
  - Improved response to track smoothly to the defined thermal and power limits.
  - Support for I^2C-based monitoring of voltage regulator temperature.
- Dynamic Power Management (DPM) defines multiple power levels for different clock and voltage domains to achieve best overall performance and idle power:
  - DPM includes intelligent firmware control to operate the different domains at the ideal operating point based on activity running in the system.
  - "Vega 10" supports DPM on most clock domains including engine, memory, data fabric, multimedia, etc.
  - Improved DPM response for performance and/or performance per watt optimization based on the type of workload.
- Adaptive Voltage and Frequency Scaling (AVFS) on graphics engine clock to optimize the V-F curve that each part operates on.
- Adaptive clock generator (also know as “Clock Stretcher”) on graphics engine clock to stretch the clock dynamically during didt/droop events. This helps reduce droop guardbands and improves performance per watt.
- Improved clock gating for better power and performance per watt efficiency on different SOC blocks.
- Electrical design current (EDC) mitigation and control using the on-die EDC controller.
- Dram self-refresh and display stutter.
- Data fabric operates at low power states when idle.

- Ultra Low Voltage (ULV) mode to optimize the SOC voltage during idle/static screen mode.
- Deep sleep on most clock domains to transition the clock to a very low frequency state during idle.
- Support for ACPI D-states and BACO (Bus Alive Core Off) state.
- Critical Temperature Fault (CTF) support for fast shutdown of the voltage regulators in the event that the GPU temperature exceeds a critical limit.
- Support for VRHOT and external thermal interrupt handling.
- Support for HBM CATTRIP handling to shut down the GPU in case of HBM memory reaching a critical temperature.

2.8 Spread-spectrum Support

2.8.1 Engine Spread-spectrum Support

Internal engine spread-spectrum support programmable from 0% to 2% down spread with modulation frequencies from 30 kHz to 33 kHz.

2.8.2 DisplayPort Internal Spread-spectrum Support

- From 0.25% to 0.5% down spread.
- Modulation frequency between 30 kHz and 33 kHz.

2.9 Internal Thermal Sensor

"Vega 10" has an integrated thermal sensor that offers the following advantages:

- Provides GPU die temperature (accuracy ± 3°C) without the need for an external chip.
- High- and low-notification limits can be defined to generate interrupts and to change power states.
- Can be used to control a fan through PWM (see Table 3–17 (p. 33)).
- A critical temperature limit can be defined to allow the system to protect the GPU from damage (see CTF in Table 3–17 (p. 33)).
- Temperature information can be provided through software (ACPI control methods) or directly through the SMBus hardware interface.

2.10 Thermal Diode

The thermal diode in "Vega 10" is a grounded collector PNP BJT. The thermal diode has two pins for its interface—DPLUS and DMINUS (see Table 3–17 (p. 33)). DPLUS connects to the emitter of the BJT while DMINUS connects to its base. The collector is tied to substrate ground.

Note:

- The thermal diode can only be used when the GPU is powered; for example, it cannot be used when in D3 cold. The 3.3-V supply has to be active for temperature sensing to work because of the ESD protection diodes.
- The ideality factor of the on-die thermal diode varies significantly with temperature and sourcing current. If a design chooses to use the on die thermal diode of the GPU coupled with an external thermal sensor chip to read the GPU temperature, the external thermal sensor chip must support and enable beta compensation.

2.11 Logo Compliance

This product complies with the Windows Logo Program requirements for all target operating systems. This includes both the current logo and future (draft) requirements that will be enforced during the lifespan of the product.

2.12 Test Capability Features

"Vega 10" has a variety of test modes and capabilities that provide a high-fault coverage and low-DPM (defect per million) ratio. It provides the following features which are implemented in the SOC:

- Full-scan implementation on the digital core logic which provides high-fault coverage through ATPG (automatic test-pattern generation) vectors, covers both the stuck-at and at-speed transition fault.
- Dedicated test logic (MBIST) for the on-chip memory macros to provide complete coverage on these modules.
- JTAG (Joint Test Action Group) test mode, fully compliant with the IEEE.
- 1149.1 standard to support test access interface and board-level connectivity test.
- Integrated hardware-diagnostic tests performed automatically upon initialization.
- Test Data Register configuration mechanism to support SCAN/MBIST and other chip-level test functions.
- Supports analog Macro at-speed loopback test to cover parts which are not covered by scan/MBIST.
- Improved access to analog Macro and PLLs to allow full evaluation and characterization of these modules.
- Integrated hardware-diagnostic tests performed automatically upon initialization.
- Scan register value dump out under security state control.

2.13 Other Features

- Support for serial-ROM video BIOS.
- Support for 32- and 64-bit operating systems based on Intel, AMD, and PowerPC CPUs.

2.14 Export Control Classification

For information on the export control classification of this product, please contact dl.exportcontrol@amd.com.

3

Signal Descriptions

This section describes the signals of "Vega 10".

The following conventions are used:

- All active low signals are shown with the suffix “B”, such as CASA0B.
- “PD” denotes a permanent internal pull down. “PD-register” denotes an internal pull down which is register controlled, and by default is turned off. “PD-reset” denotes an internal pull down which is register controlled, and by default is turned on. “PD-reset” also denotes that the internal pull down is active during reset. “PD” or “PD-reset” is not relevant when the pins are in output modes.
- To designate a group of pins that have the same pin name but are distinguished by a trailing number only, such as QSA_0, QSA_1, or QSA_2, the abbreviation “Pin name[y:x]” is used. For example, QSA_[7:0] means pins QSA_7 to QSA_0.
- In the "Vega 10" pin assignment:
  - NC or NC_*: Pins marked as NC are free pins that have no electrical connection on the GPU package.
  - RSVD: These pins should float (i.e., no electrical connection) on the PCB.

To go to a topic of interest, use the following list of linked cross-references:

3.1 Pin Assignments

Table 3–1 Pin Assignments (Left Half)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A		VDDCR_SOC	VDDCR_SOC	VDDCR_SOC		VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC
B	RSVD	DFTIO_29	VSS	DFTIO_44	DFTIO_31	DFTIO_48	VSS	DFTIO_58	DFTIO_68	VDDCR_SOC	VSS	RSVD	DFTIO_86	DFTIO_91	VDDCR_SOC	DFTIO_97	DFTIO_107	DFTIO_109	VDDCR_SOC	DFTIO_112	DFTIO_120	DFTIO_121	VDDCR_SOC
C	DFTIO_17	DFTIO_9	DFTIO_21	DFTIO_22	VSS	DFTIO_32	DFTIO_49	DFTIO_52	VSS	DFTIO_75	DFTIO_87	RSVD	VSS	DFTIO_74	DFTIO_82	DFTIO_85	VSS	DFTIO_96	DFTIO_102	DFTIO_104	VSS	DFTIO_115	DFTIO_119
D	VSS	DFTIO_18	DFTIO_27	DFTIO_13	DFTIO_33	DFTIO_39	VSS	DFTIO_36	DFTIO_47	DFTIO_70	VSS	RSVD	DFTIO_65	DFTIO_77	VDDCR_SOC	DFTIO_92	DFTIO_101	DFTIO_105	VDDCR_SOC	DFTIO_108	DFTIO_110	DFTIO_116	VDDCR_SOC
E		VSS	DFTIO_5	DFTIO_2	VSS	DFTIO_12	DFTIO_16	DFTIO_34	VSS	DFTIO_64	DFTIO_56	DFTIO_55	VSS	DFTIO_62	DFTIO_79	DFTIO_84	VSS	DFTIO_94	DFTIO_111	DFTIO_117	VSS	DFTIO_106	DFTIO_126
F	VSS	TXCFP_DPF3P	TXCFM_DPF3N	VSS	DDC1DATA	DDC1CLK	VSS	DFTIO_25	DFTIO_53	DFTIO_38	VSS	DFTIO_46	DFTIO_50	DFTIO_61	VDDCR_SOC	DFTIO_89	DFTIO_95	DFTIO_103	VDDCR_SOC	DFTIO_127	DFTIO_138	DFTIO_122	VDDCR_SOC
G	TX0P_DPF2P	TX0M_DPF2N	VSS	AUX1P	AUX1N	VSS	HPD1	DFTIO_28	VSS	DFTIO_42	DFTIO_57	DFTIO_45	VSS	DFTIO_63	DFTIO_83	DFTIO_80	VSS	DFTIO_76	DFTIO_88	DFTIO_98	VSS	DFTIO_81	DFTIO_114
H	VSS	TX1P_DPF1P	TX1M_DPF1N	VSS	VDDAN_33	VDDAN_33	VSS	DFTIO_20	DFTIO_43	DFTIO_30	VSS	DFTIO_59	DFTIO_69	DFTIO_73	VDDCR_SOC	DFTIO_60	DFTIO_71	DFTIO_67	VDDCR_SOC	DFTIO_66	DFTIO_72	DFTIO_78	VDDCR_SOC
J	TX2P_DPF0P	TX2M_DPF0N	VSS	DDC2DATA	DDC2CLK	VSS	DFTIO_0	DFTIO_26	VSS	DFTIO_35	DFTIO_37	DFTIO_41	VDDCR_SOC	DFTIO_40	DFTIO_54	VSS	VDDCR_SOC	DFTIO_90	DFTIO_100	DFTIO_99	VDDCR_SOC	DFTIO_125	DFTIO_150
K	VSS	AUX2P	AUX2N	VSS	GENERIC_HPD2	VDDAN_33	VSS	DFTIO_23	DFTIO_14	DFTIO_19	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
L	TXCEP_DPE3P	TXCEM_DPE3N	VSS	RSVD	VSS	VDDAN_33	DFTIO_7	DFTIO_3	VSS	DFTIO_24	DFTIO_1	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
M	VSS	TX3P_DPE2P	TX3M_DPE2N	VSS	VDDAN_18	VDDAN_18	VSS	DFTIO_11	DFTIO_6	DFTIO_4	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
N	TX4P_DPE1P	TX4M_DPE1N	VSS	VDDAN_18	VSS	VDDAN_18	RSVD	DFTIO_8	VSS	DFTIO_10	RSVD	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
P	VSS	TX5P_DPE0P	TX5M_DPE0N	VSS	AUX_ZVSS	GENERIC_HPD3	VSS	RSVD	DFTIO_15	RSVD	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
R	TXCDP_DPD3P	TXCDM_DPD3N	VSS	DDCAUX3P	DDCAUX3N	VSS	GENLK_CLK	GENLK_VSYNC	VSS	RSVD	RSVD	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
T	VSS	TX0P_DPD2P	TX0M_DPD2N	VSS	SWAPLOCKA	SWAPLOCKB	VSS	GPIO_0	GPIO_SVD0	RSVD	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
U	TX1P_DPD1P	TX1M_DPD1N	VSS	RSVD	RSVD	VSS	GPIO_1	GPIO_SVT0	VSS	RSVD	RSVD	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
V	VSS	TX2P_DPD0P	TX2M_DPD0N	VSS	GENERIC_HPD4	GPIO_9_ROMSO	GPIO_2	VSS	GPIO_SVC0	INTCRACKMONGLL	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
W	TXCCP_DPC3P	TXCCM_DPC3N	VSS	DDCAUX4P	DDCAUX4N	VSS	GPIO_7_ROMSCK	GPIO_8_ROMSI	VSS	RSVD	RSVD	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
Y	VSS	TX3P_DPC2P	TX3M_DPC2N	VSS	VDD_18	VDD_18	GPIO_10_ROMCSB	VSS	RSVD	INTCRACKMONGLR	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
AA	TX4P_DPC1P	TX4M_DPC1N	VSS	RSVD	VDD_18	VSS	RSVD	TRST_L	VSS	RSVD	RSVD	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
AB	VSS	TX5P_DPC0P	TX5M_DPC0N	VSS	VDD_18	VDD_18	VSS	TDO	TDI	RSVD	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS
AC	TXCBP_DPB3P	TXCBM_DPB3N	VSS	GENERIC_HPD5	VSS	VDD_18	TMS	TCK	VSS	RSVD	RSVD	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC
AD	VSS	TX0P_DPB2P	TX0M_DPB2N	VSS	DDCAUX5P	DDCAUX5N	VSS	TESTEN	XTRIG6	RSVD	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC
AE	TX1P_DPB1P	TX1M_DPB1N	VSS	GENERIC_HPD6	VSS	VDD_18	GPIO_5	GPIO_6	VSS	INTCRACKMONDA	RSVD	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VSS	VSS	VSS
AF	VSS	TX2P_DPB0P	TX2M_DPB0N	VSS	DDCAUX6P	DDCAUX6N	VSS	VDDAN_Q_EFUSE	VDDAN_Q_EFUSE	RSVD	VSS	VSS	VSS	VSS	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VSS	VSS	VSS
AG	TXCAP_DPA3P	TXCAM_DPA3N	VSS	VDD_18	VDD_18	DP_ZVSS	GPIO_4	GPIO_3	XTRIG7	VDDCR_BACO	VDDCR_BACO	VSS	VSS	VSS	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC
AH	VSS	TX3P_DPA2P	TX3M_DPA2N	VSS	VDD_18	DP_ZVDD_08	VSS	VSS	VDDCR_BACO	VDDCR_BACO	VSS	VSS	VSS	VSS	VSS	VSS	FB_VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC
AJ	TX4P_DPA1P	TX4M_DPA1N	VSS	RSVD	RSVD	VSS	ANALOGIO	RSVD	VSS	RSVD	TEST_PG	VSS	VSS	RSVD	HBMA_DAP_49	FB_VSS_A	HBMA_DAP_32	HBMA_DAP_28	VSS	HBMA_DAP_12	HBMA_DAP_7	VSS	HBMA_DAP_17
AK	VSS	TX5P_DPA0P	TX5M_DPA0N	VSS	PCIE_ZVSS	VSS	RSVD	VDD_080_EFUSE	VDD_080_EFUSE	RSVD	VSS	VSS	VSS	HBMA_DAP_59	HBMA_DAP_46	FB_VDDCI_MEM	HBMA_DAP_38	VSS	HBMA_DAP_23	HBMA_DAP_21	VSS	HBMA_DAP_14	HBMA_DAP_19
AL	VSS	GENERICA	VSS	GPIO_11	GPIO_12	RSVD	VDD_080	RSVD	VSS	TS_A	RSVD	VSS	VSS	HBMA_DAP_58	RSVD	VSS	VDDCI_MEM	HBMA_DAP_26	HBMA_DAP_41	VDDCI_MEM	HBMA_DAP_13	HBMA_DAP_11	VDDCI_MEM
AM	XTALIN	VSS	XTALOUT	VSS	GPIO_14	GPIO_13	VSS	VDD_080	DBREQ_L	SDA	VSS	VSS	VSS	RSVD	MTESTA	VSS	HBMA_DAP_39	HBMA_DAP_40	VDDCI_MEM	HBMA_DAP_27	HBMA_DAP_22	VDDCI_MEM	HBMA_DAP_35
AN	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VSS	RSVD	VSS	SCL	RSVD	RSVD	VSS	RSVD	HBMA_DAP_52	VSS	HBMA_DAP_51	VSS	HBMA_DAP_50	HBMA_DAP_34	VSS	HBMA_DAP_15	HBMA_DAP_42
AP	OSC_GAIN0	OSC_GAIN1	OSC_GAIN2	RSVD	RSVD	RSVD	VSS	VDD_080	RSVD	RSVD	VSS	VSS	VSS	HBMA_DAP_53	HBMA_DAP_56	VDDIO_MEM	VSS	VDDCR_HBM	VDDCR_HBM	VSS	VDDCR_HBM	VDDCR_HBM	VSS
AR	BP_0	BP_1	VSS	GPIO_15	GPIO_16	GPIO_17	VSS	RSVD	VSS	RSVD	RSVD	VSS	VSS	HBMA_DAP_57	VREFEXTA	VSS	HBMA_DAP_43	HBMA_DAP_54	VDDIO_MEM	HBMA_DAP_31	HBMA_DAP_44	VDDIO_MEM	HBMA_DAP_36
AT	BP_3	BP_2	VSS	GPIO_18	GPIO_19	GPIO_20	VSS	VDD_080	RSVD	RSVD	VSS	MACO_EN	VSS	HBMA_DAP_55	VSS	VDDCR_HBM	VDDIO_MEM	VDDIO_MEM	HBMA_DAP_48	HBMA_DAP_47	VDDIO_MEM	HBMA_DAP_45	HBMA_DAP_37
AU	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VSS	RSVD	VSS	VSS	BL_ENABLE	RSVD	PX_EN	VSS	VDDCR_HBM	VDDIO_MEM	VSS	VDDCR_HBM	VDDCR_HBM	VSS
AV	RSVD	RSVD	RSVD	VDD_080	VSS	VSS	VDD_080	RSVD	VSS	VDD_080	VSS	RSVD	RSVD	GENERICB	TEST_PG_BACO	BL_PWM_DIM	DIGON	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
AW	RSVD	RSVD	VDD_080	VSS	VSS	VDD_080	RSVD	VSS	VDD_080	RSVD	VSS	RSVD	RSVD	VSS	RSVD	RSVD	VSS	VSS	VSS	VSS	VSS	VSS	RSVD
AY	PINSTRAP_7	PINSTRAP_6	PINSTRAP_5	VSS	PCIE_REFCLKP	PCIE_REFCLKN	VSS	PCIE_TX2P	PCIE_TX2N	VSS	PCIE_TX5P	PCIE_TX5N	VSS	PCIE_TX8P	PCIE_TX8N	VSS	PCIE_TX11P	PCIE_TX11N	VSS	PCIE_TX14P	PCIE_TX14N	VSS	RSVD
BA		PINSTRAP_4	PINSTRAP_3	RSVD	VSS	VSS	PCIE_TX1P	PCIE_TX1N	VSS	PCIE_TX4P	PCIE_TX4N	VSS	PCIE_TX7P	PCIE_TX7N	VSS	PCIE_TX10P	PCIE_TX10N	VSS	PCIE_TX13P	PCIE_TX13N	VSS	VSS	RSVD
BB	PINSTRAP_2	PINSTRAP_1	PINSTRAP_0	VSS	VSS	PCIE_TX0P	PCIE_TX0N	VSS	PCIE_TX3P	PCIE_TX3N	VSS	PCIE_TX6P	PCIE_TX6N	VSS	PCIE_TX9P	PCIE_TX9N	VSS	PCIE_TX12P	PCIE_TX12N	VSS	PCIE_TX15P	PCIE_TX15N	VSS
BC	SMBDAT	SMBCLK	RSVD	VSS	PCIE_RX0P	PCIE_RX0N	VSS	PCIE_RX3P	PCIE_RX3N	VSS	PCIE_RX6P	PCIE_RX6N	VSS	PCIE_RX9P	PCIE_RX9N	VSS	PCIE_RX12P	PCIE_RX12N	VSS	PCIE_RX15P	PCIE_RX15N	VSS	RSVD
BD	VSS	WAKEB	PERSTB	RSVD	VSS	VSS	PCIE_RX2P	PCIE_RX2N	VSS	PCIE_RX5P	PCIE_RX5N	VSS	PCIE_RX8P	PCIE_RX8N	VSS	PCIE_RX11P	PCIE_RX11N	VSS	PCIE_RX14P	PCIE_RX14N	VSS	RSVD	VSS
BE		VSS	CLKREQB	VSS		PCIE_RX1P	PCIE_RX1N	VSS	PCIE_RX4P	PCIE_RX4N	VSS	PCIE_RX7P	PCIE_RX7N	VSS	PCIE_RX10P	PCIE_RX10N	VSS	PCIE_RX13P	PCIE_RX13N	VSS	VSS	REFCLKP	REFCLKN
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

Table 3–2 Pin Assignments (Right Half)

24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	
VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC		VDDCR_SOC	VDDCR_SOC	VDDCR_SOC		A
DFTIO_135	DFTIO_136	DFTIO_143	VDDCR_SOC	DFTIO_152	DFTIO_158	DFTIO_161	VDDCR_SOC	DFTIO_165	DFTIO_166	DFTIO_174	VDDCR_SOC	DFTIO_210	DFTIO_211	DFTIO_203	VSS	DFTIO_201	DFTIO_202	DFTIO_209	VSS	DFTIO_187	VDDCR_SOC	B
DFTIO_129	VSS	DFTIO_118	DFTIO_131	DFTIO_139	VSS	DFTIO_153	DFTIO_133	DFTIO_147	VSS	DFTIO_151	DFTIO_167	DFTIO_175	VSS	DFTIO_169	DFTIO_222	DFTIO_217	VSS	DFTIO_204	DFTIO_182	DFTIO_189	VDDCR_SOC	C
DFTIO_128	DFTIO_132	DFTIO_146	VDDCR_SOC	DFTIO_137	DFTIO_142	DFTIO_154	VDDCR_SOC	DFTIO_162	DFTIO_179	DFTIO_190	VDDCR_SOC	DFTIO_149	DFTIO_181	DFTIO_164	VSS	DFTIO_172	DFTIO_192	DFTIO_180	VSS	DFTIO_186	VDDCR_SOC	D
DFTIO_141	VSS	DFTIO_176	DFTIO_177	DFTIO_157	VSS	DFTIO_148	DFTIO_163	DFTIO_173	VSS	DFTIO_208	DFTIO_214	DFTIO_221	VSS	DFTIO_219	DFTIO_216	DFTIO_228	VSS	DFTIO_194	DFTIO_199	DFTIO_188		E
DFTIO_145	DFTIO_134	DFTIO_159	VDDCR_SOC	DFTIO_168	DFTIO_183	DFTIO_196	VDDCR_SOC	DFTIO_185	DFTIO_220	DFTIO_206	VDDCR_SOC	DFTIO_254	DFTIO_243	DFTIO_235	VSS	DFTIO_200	DFTIO_229	DFTIO_195	VSS	DFTIO_215	VDDCR_SOC	F
DFTIO_93	VSS	DFTIO_123	DFTIO_144	DFTIO_130	VSS	DFTIO_171	DFTIO_156	DFTIO_212	VSS	DFTIO_252	DFTIO_234	DFTIO_227	VSS	DFTIO_257	DFTIO_245	DFTIO_244	VSS	DFTIO_223	DFTIO_224	DFTIO_205	VDDCR_SOC	G
DFTIO_155	DFTIO_170	DFTIO_113	VDDCR_SOC	DFTIO_178	DFTIO_191	DFTIO_198	VDDCR_SOC	DFTIO_290	DFTIO_281	DFTIO_238	VDDCR_SOC	DFTIO_218	DFTIO_207	DFTIO_269	VDDCR_SOC	DFTIO_272	DFTIO_249	DFTIO_226	VDDCR_SOC	DFTIO_225	VDDCR_SOC	H
DFTIO_160	VDDCR_SOC	DFTIO_124	DFTIO_140	DFTIO_184	VDDCR_SOC	DFTIO_197	DFTIO_213	DFTIO_232	VDDCR_SOC	DFTIO_247	DFTIO_193	DFTIO_255	VSS	DFTIO_264	DFTIO_256	DFTIO_259	VSS	DFTIO_242	DFTIO_230	DFTIO_231	VDDCR_SOC	J
VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	DFTIO_265	DFTIO_286	VDDCR_SOC	DFTIO_246	DFTIO_239	DFTIO_241	VDDCR_SOC	DFTIO_233	VDDCR_SOC	K
VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	DFTIO_280	DFTIO_289	DFTIO_276	VDDCR_SOC	DFTIO_248	DFTIO_240	DFTIO_237	VDDCR_SOC	L
VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	DFTIO_275	DFTIO_310	VDDCR_SOC	DFTIO_282	DFTIO_261	DFTIO_253	VDDCR_SOC	DFTIO_236	VDDCR_SOC	M
VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DFTIO_320	DFTIO_300	DFTIO_287	VSS	DFTIO_260	DFTIO_250	DFTIO_251	VDDCR_SOC	N
VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VSS	VSS	VSS	VSS	DFTIO_295	DFTIO_324	VSS	DFTIO_301	DFTIO_288	DFTIO_267	VSS	DFTIO_258	VDDCR_SOC	P
VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	DFTIO_315	DFTIO_270	DFTIO_309	VDDCR_SOC	DFTIO_284	DFTIO_262	DFTIO_263	VDDCR_SOC	R
VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	TEST6	DFTIO_322	VDDCR_SOC	DFTIO_303	DFTIO_277	DFTIO_268	VDDCR_SOC	DFTIO_285	VDDCR_SOC	T
VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DFTIO_278	DFTIO_279	DFTIO_308	VSS	DFTIO_271	DFTIO_298	DFTIO_296	VDDCR_SOC	U
VSS	VDDCR_SOC	VDDCR_SOC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INTCRACKMONGUL	DFTIO_283	VSS	DFTIO_299	DFTIO_273	DFTIO_274	VSS	DFTIO_266	VDDCR_SOC	V
VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	DFTIO_291	DFTIO_292	DFTIO_293	VDDCR_SOC	DFTIO_304	DFTIO_306	DFTIO_297	VDDCR_SOC	W
VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	INTCRACKMONGUR	DFTIO_294	VDDCR_SOC	DFTIO_316	DFTIO_323	DFTIO_305	VDDCR_SOC	DFTIO_302	VDDCR_SOC	Y
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DFTIO_329	DFTIO_318	DFTIO_321	VSS	DFTIO_312	DFTIO_313	DFTIO_307	VDDCR_SOC	AA
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DFTIO_332	DFTIO_335	VSS	DFTIO_317	DFTIO_314	DFTIO_325	VSS	DFTIO_311	VDDCR_SOC	AB
VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	DFTIO_334	DFTIO_326	DFTIO_319	VDDCR_SOC	DFTIO_333	DFTIO_330	DFTIO_328	VDDCR_SOC	AC
VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	RSVD	RSVD	VDDCR_SOC	RSVD	DFTIO_327	DFTIO_331	VDDCR_SOC	RSVD	VDDCR_SOC	AD
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RSVD	RSVD	RSVD	VSS	RSVD	RSVD	RSVD	VDDCR_SOC	AE
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RSVD	RSVD	VSS	RSVD	RSVD	RSVD	VSS	RSVD	VDDCR_SOC	AF
VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	RSVD	RSVD	RSVD	VDDCR_SOC	RSVD	RSVD	RSVD	VDDCR_SOC	AG
VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	DFTIO_370	RSVD	VDDCR_SOC	RSVD	RSVD	RSVD	VDDCR_SOC	RSVD	VDDCR_SOC	AH
HBMA_DAP_8	VSS	HBMA_DAP_6	HBMA_DAP_0	VSS	HBMB_DAP_47	HBMB_DAP_41	VSS	HBMB_DAP_30	HBMB_DAP_24	VSS	HBMB_DAP_11	HBMB_DAP_1	VSS	DFTIO_383	DFTIO_378	DFTIO_342	VSS	RSVD	DFTIO_381	RSVD	VDDCR_SOC	AJ
VSS	HBMA_DAP_9	HBMA_DAP_1	VSS	HBMB_DAP_59	HBMB_DAP_55	VSS	HBMB_DAP_44	HBMB_DAP_31	VSS	HBMB_DAP_14	HBMB_DAP_10	VSS	VSS	RSVD	VSS	RSVD	DFTIO_377	DFTIO_360	VSS	DFTIO_362	VDDCR_SOC	AK
HBMA_DAP_20	HBMA_DAP_16	VDDCI_MEM	HBMA_DAP_5	HBMB_DAP_58	VDDCI_MEM	HBMB_DAP_50	HBMB_DAP_39	VDDCI_MEM	HBMB_DAP_21	HBMB_DAP_17	VDDCI_MEM	HBMB_DAP_7	HBMB_DAP_0	RSVD	DFTIO_382	DFTIO_371	VDDCR_SOC	DFTIO_369	DFTIO_373	DFTIO_380	VDDCR_SOC	AL
HBMA_DAP_29	VDDCI_MEM	HBMA_DAP_4	HBMA_DAP_3	VDDCI_MEM	HBMB_DAP_48	HBMB_DAP_45	VDDCI_MEM	HBMB_DAP_27	HBMB_DAP_23	VDDCI_MEM	HBMB_DAP_13	HBMB_DAP_3	RSVD	RSVD	VDDCR_SOC	DFTIO_336	DFTIO_372	DFTIO_337	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	AM
VSS	HBMA_DAP_18	HBMA_DAP_10	VSS	HBMB_DAP_54	HBMB_DAP_53	VSS	HBMB_DAP_38	HBMB_DAP_33	VSS	HBMB_DAP_16	HBMB_DAP_6	VSS	MTESTB	RSVD	DFTIO_363	DFTIO_368	VSS	DFTIO_339	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	AN
VDDCR_HBM	VDDCR_HBM	VSS	VDDCR_HBM	VDDCR_HBM	VSS	VDDIO_MEM	HBMB_DAP_37	VSS	VDDCR_HBM	HBMB_DAP_22	VSS	HBMB_DAP_2	HBMB_DAP_5	RSVD	DFTIO_379	DFTIO_374	DFTIO_375	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	AP
HBMA_DAP_30	VDDIO_MEM	HBMA_DAP_25	HBMA_DAP_2	VDDIO_MEM	HBMB_DAP_49	HBMB_DAP_42	VDDIO_MEM	HBMB_DAP_32	HBMB_DAP_28	VDDCR_HBM	HBMB_DAP_9	VREFEXTB	RSVD	RSVD	DFTIO_364	DFTIO_365	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	DFTIO_341	AR
VDDIO_MEM	HBMA_DAP_33	HBMA_DAP_24	VDDIO_MEM	HBMB_DAP_57	HBMB_DAP_52	VDDIO_MEM	HBMB_DAP_43	HBMB_DAP_26	VDDIO_MEM	HBMB_DAP_18	HBMB_DAP_8	RSVD	TEMPINRETURN	VSS	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	DFTIO_355	DFTIO_340	DFTIO_338	AT
VDDIO_MEM	RSVD	VSS	RSVD	HBMB_DAP_56	VSS	HBMB_DAP_46	HBMB_DAP_36	VSS	HBMB_DAP_25	HBMB_DAP_12	VSS	INTCRACKMONDB	TEMPIN	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	VDDCR_SOC	DFTIO_357	DFTIO_358	DFTIO_376	VSS	AU
VDDIO_MEM	VSS	VDDIO_MEM	VDDIO_MEM	VSS	HBMB_DAP_51	HBMB_DAP_40	VSS	HBMB_DAP_34	HBMB_DAP_19	VSS	HBMB_DAP_15	RSVD	VSS	RSVD	RSVD	DFTIO_344	DFTIO_366	DFTIO_367	VSS	DFTIO_356	RSVD	AV
RSVD	VDDCR_HBM	RSVD	RSVD	VDDCR_HBM	RSVD	VDDIO_MEM	HBMB_DAP_35	HBMB_DAP_29	VDDIO_MEM	HBMB_DAP_20	HBMB_DAP_4	VDDIO_MEM	VDDCR_HBM	RSVD	RSVD	DFTIO_352	VSS	DFTIO_347	DFTIO_345	DFTIO_349	VSS	AW
VDDIO_MEM	PLLCHARZ1_L	PLLCHARZ1_H	VDDCR_HBM	FB_VSSB	FB_VDDIO_MEM_GPU	RSVD	RSVD	VDDIO_MEM	RSVD	RSVD	VDDIO_MEM	RSVD	RSVD	VDDIO_MEM	VSS	DFTIO_359	DFTIO_351	DFTIO_346	VSS	DFTIO_353	DFTIO_343	AY
RSVD	RSVD	RSVD	VSS	FB_VDDIO_MEM_HBM	FB_VDDCR_HBM	RSVD	VSS	RSVD	VDDCR_HBM	VSS	RSVD	RSVD	VSS	RSVD	RSVD	DFTIO_354	VSS	DFTIO_361	DFTIO_348	DFTIO_350		BA
RSVD	RSVD	RSVD	RSVD	VSS	VSS	VSS	RSVD	RSVD	VDDIO_MEM	DPLUS	VDDIO_MEM	VDDIO_MEM	RSVD	RSVD	VDDIO_MEM	RSVD	RSVD	VSS	RSVD	VSS	VSS	BB
RSVD	VSS	RSVD	RSVD	RSVD	PROCHOT_L	VSS	RSVD	VSS	RSVD	DMINUS	VSS	RSVD	RSVD	VSS	RSVD	RSVD	VSS	INTCRACKMONPDG	INTCRACKMONP	VSS	VSS	BC
RSVD	VSS	VPP	RSVD	RSVD	FANOUT	DDCVGACLK	ALERT_L	RSVD	PUMPOUT	VSS	RSVD	RSVD	VSS	RSVD	RSVD	VSS	RSVD	RSVD	VSS	VSS	VSS	BD
RSVD	VSS	VPP	VPP	VSS	FANIN	DDCVGADATA	CTF	RSVD	PUMPIN	VSS	RSVD	RSVD	VSS	RSVD	VSS	RSVD		VSS	VSS	VSS		BE
24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	

3.2 PCI Express® Bus Interface

For more information on signal definitions and electrical requirements, refer to the *PCI Express® Card Electromechanical 3.0 Specification* and *PCI Express Base 3.0 Specification*.

Note:

- "Vega 10" supports ×16 lane reversal, where the receivers on lanes 0 to 15 of the graphics endpoint are mapped to the transmitter on lanes 15 down to 0 of the root complex. If ×16 lane reversal is employed, both the receive and transmit lanes must be reversed. In addition, polarity inversion is supported, such as when the + of the differential pair is connected to the - at the root complex.
- 220-nF AC-coupling capacitors are required.

Table 3–3 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTB	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3. A buffered reset signal dedicated to the GPU is required.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[15:0]P/N	O	PCI Express transmitter output data channel TX[15:0] (+/-). Differential serial data transmitted up to 8.0-GT/s bit rate.
PCIE_RX[15:0]P/N	I	PCI Express receiver input data channel RX[15:0] (+/-). Differential serial data received up to 8.0-GT/s bit rate.
PCIE_ZVSS	I/O	Connect to VSS through a 200-Ω (1% tolerance) 100 ppm/C resistor. Resistor parasitic capacitance <10 pF.
CLKREQB	I/O	CLKREQB only: CLKREQB is an open drain output from the GPU and an input to the platform which can be used to request the PCIe® reference clock to GPU on or off. L1 PM Substates: CLKREQB is a bi-directional open drain that can be asserted by either the GPU or the platform to initiate an L1 exit.
WAKEB	I	Reserved. Do not connect on the PCB.

3.3 Memory Interface (HBM)

Table 3–4 Memory Interface

Pin Name	I/O	Description
HBMA_DAP_[0:59] HBMB_DAP_[0:59]	I/O	Debugging purposes, can be left floating.
VREFEXTA VREFEXTB	I/O	External voltage reference for HBM. 0.5 × VDDIO_MEM Two 100-Ω 1% resistors can be used to form the divider on each pin. Filter capacitor is needed to ensure AC noise is within ±10 mV.
MTESTA MTESTB	O	Reserved. Provide test pads on the PCB.

3.4 Display Configuration Overview

"Vega 10" has six display links, A to F.

Table 3–5 Display Configuration Overview for Links A, B, C, D, E, and F

Pin Name	Possible Display Configurations	
TX[5:3]P/M_DPA[0:2]P/N **TXCAP/M_DPA3P/N**	Single-link DisplayPort/ TMDS	DisplayPort can be connected to any of links A, B, C, D, E, or F. The six links are independent and can be simultaneously active. HDMI or single-link DVI can be connected to any of the links (A, B, C, D, E, or F). For native dual-link DVI support, contact AMD.
TX[2:0]P/M_DPB[0:2]P/N **TXCBP/M_DPB3P/N**	Single-link DisplayPort/ TMDS	
TX[5:3]P/M_DPC[0:2]P/N **TXCCP/M_DPC3P/N**	Single-link DisplayPort/ TMDS	
TX[2:0]P/M_DPD[0:2]P/N **TXCDP/M_DPD3P/N**	Single-link DisplayPort/ TMDS	
TX[5:3]P/M_DPE[0:2]P/N **TXCEP/M_DPE3P/N**	Single-link DisplayPort/ TMDS	
TX[2:0]P/M_DPF[0:2]P/N **TXCFP/M_DPF3P/N**	Single-link DisplayPort/ TMDS	

3.5 Integrated HDMI™/TMDS Interface

"Vega 10" has six display links, A to F.

Note:

- The maximum pixel clock rate is 594 MHz on direct connectors. The GPU and HDMI™ connector are on the same PCB with a maximum trace length of 127 mm or 5 inches, and may be affected by TMDS signals layout and trace lengths.
- For unused interfaces, all signal outputs can be unconnected. AUX_ZVSS, DP_ZVDD_08, and DP_ZVSS should always be connected.

Please refer to the *Digital Visual Interface (DVI) 1.0 Specification* and the *High-Definition Multimedia Interface (HDMI) Specification* for additional details.

Table 3–6 Integrated HDMI™/TMDS Interface

Pin Name	Type	Description
TX[5:3]P/M_DPA[0:2]P/N **TX[2:0]P/M_DPB[0:2]P/N** **TX[5:3]P/M_DPC[0:2]P/N** **TX[2:0]P/M_DPD[0:2]P/N** **TX[5:3]P/M_DPE[0:2]P/N** **TX[2:0]P/M_DPF[0:2]P/N**	O	TMDS data pairs (+/-). Transmitting at a bit rate of 10× pixel clock, up to 594-MHz pixel clock. A 100-nF capacitor is required on each differential signal placed near the connector. A 500-Ω resistor to ground is required on each differential-signal line. One FET is needed to disconnect the path from the 500-Ω resistors to ground when the system is off and the panel is on.
TXCAP/M_DPA3P/N **TXCBP/M_DPB3P/N** **TXCCP/M_DPC3P/N** **TXCDP/M_DPD3P/N** **TXCEP/M_DPE3P/N** **TXCFP/M_DPF3P/N**	O	TMDS clock channels (+/-). A 100-nF capacitor is required on each differential signal placed near the connector. A 500-Ω resistor to ground is required on each differential-signal line. One FET is needed to disconnect the path from the 500-Ω resistors to ground when the system is off and the panel is on.
DDC[2:1]CLK **DDC[2:1]DATA** **DDCAUX[6:3]N** **DDCAUX[6:3]P**	I/O	Differential signals for HDMI/TMDS DDC. For more details, see Table 3–14 (p. 31). NOT 5-V tolerant.
AUX_ZVSS	A	Analog calibration. Connect to VSS through a 150-Ω (1%) resistor.
DP_ZVDD_08	A	Analog calibration. Connect to VDD_080 through a 200-Ω (1%) resistor.
DP_ZVSS	A	Analog calibration. Connect to GND through a 200-Ω (1%) resistor.

Note: For native dual-link DVI support, contact AMD.

3.6 DisplayPort

Note: If this interface is not used, all signal outputs can be unconnected. AUX_ZVSS, DP_ZVDD_08, and DP_ZVSS should always be connected.

"Vega 10" supports six DisplayPort links.

The GPU and DisplayPort connector are on the same PCB with a maximum trace length of 127 mm or 5 inches.

Please refer to the *DisplayPort Standard Version 1.4* for additional details.

Table 3–7 DisplayPort Interface

Pin Name	Type	Description
TX[5:3]P/M_DPA[0:2]P/N **TXCAP/M_DPA3P/N**	O	DisplayPort (DPA) differential signals. DPA can be configured as a DisplayPort link. A 100-nF capacitor is required on each differential signal placed near the connector.
TX[2:0]P/M_DPB[0:2]P/N **TXCBP/M_DPB3P/N**	O	DisplayPort (DPB) differential signals. DPB can be configured as a DisplayPort link. A 100-nF capacitor is required on each differential signal placed near the connector.
TX[5:3]P/M_DPC[0:2]P/N **TXCCP/M_DPC3P/N**	O	DisplayPort (DPC) differential signals. DPC can be configured as a DisplayPort link. A 100-nF capacitor is required on each differential signal placed near the connector.
TX[2:0]P/M_DPD[0:2]P/N **TXCDP/M_DPD3P/N**	O	DisplayPort (DPD) differential signals. DPD can be configured as a DisplayPort link. A 100-nF capacitor is required on each differential signal placed near the connector.
TX[5:3]P/M_DPE[0:2]P/N **TXCEP/M_DPE3P/N**	O	DisplayPort (DPE) differential signals. DPE can be configured as a DisplayPort link. A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector.
TX[2:0]P/M_DPF[0:2]P/N **TXCFP/M_DPF3P/N**	O	DisplayPort (DPF) differential signals. DPF can be configured as a DisplayPort link. A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector.
AUX[2:1]P/N **DDCAUX[6:3]N** **DDCAUX[6:3]P**	I/O	DisplayPort auxiliary differential signals. See Table 3–14 (p. 31)
AUX_ZVSS	A	Analog calibration. Connect to VSS through a 150-Ω (1%) resistor.
DP_ZVDD_08	A	Analog calibration. Connect to VDD_080 through a 200-Ω (1%) resistor.
DP_ZVSS	A	Analog calibration. Connect to GND through a 200-Ω (1%) resistor.

3.7 Hardware I^2 C Interface

Table 3–8 Hardware IC Interface

Pin Name	I/O	Description
SCL	I/O (VDDAN_33)	I^{2}C clock. **Note:** Can be left unconnected if not used. Frequency: Up to 100 KHz I^{2}C standard; Up to 400 KHz fast; and up to 1 MHz fast mode plus.
SDA	I/O (VDDAN_33)	I^{2}C clock. **Note:** Can be left unconnected if not used. Frequency: Up to 100 KHz I^{2}C standard; Up to 400 KHz fast; and up to 1 MHz fast mode plus.

3.8 Serial Flash Interface

Configuration straps must be set to identify the appropriate ROM type. See Configuration Straps (p. 37).

Table 3–9 Serial Flash Interface

Pin Name	Type	PD/PU	Description
GPIO_9_ROMSO	I (VDDAN_33)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output.
GPIO_8_ROMSI	O (VDDAN_33)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_7_ROMSCK	O (VDDAN_33)	PD-reset	Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMCSB	O (VDDAN_33)	PU-reset	BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations.

3.9 General Purpose I/O Interface

Table 3–10 General Purpose I/O Interface

Pin Name	Type	PD/PU	Description
GPIO_0	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O. Can be used as interrupt input to trigger fast power reduction from GPU when system power source is switched from AC adapter to battery. Can be left unconnected if not used.
GPIO_1	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O. Can be unconnected if not used.
GPIO_2	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O. Can be unconnected if not used.
GPIO_3	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O. Can be unconnected if not used.
GPIO_4	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O. Can be unconnected if not used.
GPIO_5	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O. Can be used as VRHOT interrupt to the GPU indicating thermal overload of the regulator. Can be unconnected if not used.
GPIO_6	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O. Can be used as an alternative input for VRHOT interrupt to the GPU indicating thermal overload of the regulator. Can be unconnected if not used.
GPIO_7_ROMSCK	I/O 3.3V (VDDAN_33)	PD-reset	For designs that have dedicated ROM for video BIOS, it serves as the serial ROM clock. See Table 3–9 (p. 26) for serial ROM usage.
GPIO_8_ROMSI	I/O 3.3V (VDDAN_33)	PD-reset	For designs that have dedicated ROM for video BIOS, it serves as the serial ROM input. See Table 3–9 (p. 26) for serial ROM usage.
GPIO_9_ROMSO	I/O 3.3V (VDDAN_33)	PD-reset	For designs that have dedicated ROM for video BIOS, it serves as the serial ROM output. See Table 3–9 (p. 26) for serial ROM usage.
GPIO_10_ROMCSB	I/O 3.3V (VDDAN_33)	PU-reset	For designs that have dedicated ROM for video BIOS, it serves as the serial ROM chip-select. See Table 3–9 (p. 26) for serial ROM usage. Also serves as pin strap. See Table 3–24 (p. 38) for pin strap definition.
GPIO_11	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O and pin strap. See Table 3–24 (p. 38) for pin strap definition.

Pin Name	Type	PD/PU	Description
GPIO_12	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O and pin strap. See Table 3–24 (p. 38) for pin strap definition.
GPIO_13	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O and pin strap. See Table 3–24 (p. 38) for pin strap definition.
GPIO_14	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O.
GPIO_15	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O and pin strap. See Table 3–24 (p. 38) for pin strap definition.
GPIO_16	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O and pin strap. See Table 3–24 (p. 38) for pin strap definition.
GPIO_17	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O and pin strap. See Table 3–24 (p. 38) for pin strap definition.
GPIO_18	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O and pin strap. Can be unconnected if not used. See Table 3–24 (p. 38) for pin strap definition
GPIO_19	I/O 3.3V (VDDAN_33)	PD-reset	General purpose I/O and pin strap. See Table 3–24 (p. 38) for pin strap definition.
GPIO_20	I/O 3.3V (VDDAN_33)	PD-reset	Do not connect on the PCB. Provide a test pad.

Note:

1. During ramp-up of the VDDAN_33 power rail, all GPIOs are undefined and a voltage bump may appear momentarily (less than 200 mV).
2. Internal PU or PD is effective after VDDCR_SOC is at ready state. Before VDDCR_SOC is ready, the GPIOs are of Hi-Z state.
3. All GPIOs are configured as input by default after VDDCR_SOC is at ready state. GPIOs can be programmed as output by the video BIOS or driver.
4. For GPIOs that serve as pin straps, any external circuits using them must not conflict with the logic level required by the strap after power up until PCIe reset gets de-asserted.
5. See Configuration Straps (p. 37) for more information on pin strap configurations.

3.10 AMD SVI2 Master Interface

Table 3–11 AMD SVI2 Master Interface

Pin Name	Type	PD/PU	Description
GPIO_SVC0	I/O 1.8 V (VDDAN_18)	On-die PU	Serial VID clock. Push-pull clock output for the SVI2 data bus; driven by the GPU. Point-to-point connection to the SVI2 voltage regulator controller.
GPIO_SVD0	I/O 1.8 V (VDDAN_18)	On-die PD	Serial VID data. Push-pull data output for the SVI2 data bus; driven by the GPU. Sets the voltage, power-state indicator, load-line slope, and voltage offsets for two voltage rails. Point-to-point connection to the SVI2 voltage regulator controller.
GPIO_SVT0	I/O 1.8 V (VDDAN_18)	-	Serial VID telemetry. Push-pull data input driven by the SVI2 voltage regulator controller. Continuously streams the voltage and current telemetry information to the GPU. Also provides an indication when positive voltage transitions are complete (VOTFC).
Note: On "Vega 10", the boot voltage of the SVI2 regulator is 0.9 V controlled by the GPU; overwriting of boot-VID on the PCB is not allowed. If the second domain of the SVI2 regulator is used to power a GPU rail (e.g., VDDCR_HBM/VDDIO_MEM) that cannot work with 0.9 V, contact AMD for alternative solutions.			

3.11 Panel Control Interface

Note: All signals in this interface can be unconnected if not used. This interface may be used for eDP panels.

Table 3–12 Panel Control Interface

Pin Name	Type	PD/PU	Description
DIGON	O 3.3 V (VDDAN_33)	PD	Controls panel digital power on/off. **Note:** External pull-down resistor is recommended.
BL_PWM_DIM	O 3.3 V (VDDAN_33)	PD	LCD PWM (Pulse Width Modulated) output for adjustment of LCD brightness. Active high. BL_PWM_DIM can be used to control backlight on/off (backlight enable) by setting BL_PWM_CNTL.BL_PWM_EN = 0. **Note:** External pull-down resistor is recommended.
BL_ENABLE	I/O 3.3 V (VDDAN_33)	PD-reset	Controls backlight on/off. Active high. **Note:** External pull-down resistor is recommended.

3.12 Global Swap Lock on Multiple GPUs

Global swap lock is used to synchronize the timing and surface flip for multiple display pipes on multiple GPUs.

If this feature is not required, the following signals can be used as 3.3-V GPIOs or left unconnected on the PCB.

Table 3–13 Global Swap Lock on Multiple GPUs

Pin Name	Type	PD/ PU	Description
GENLK_CLK	I/O 3.3 V (VDDAN_33)	PD	Reference-clock input for the display PLLs (including the DCPLL and pixel PLLs) received from the framelock/genlock interface. **Note:** Can be unconnected if not used.
GENLK_VSYNC	I/O 3.3 V (VDDAN_33)	PD	Frame-timing indicator. Output to the framelock/genlock interface.
SWAPLOCKA	Open drain 3.3 V	-	(Optional) Used in a multiple GPU design with multiple display outputs to allow all displays in group A to update at the same time and have synchronous left/right stereo timing. In a multiple GPU design where displays are connected to more than one GPU, connect SWAPLOCKA from all GPUs together with an external 10-kΩ pull-up resistor. GPU genlock is needed, either via a genlock system or by feeding all GPUs with the same reference clock. Connecting SWAPLOCKB is preferred but not required.
SWAPLOCKB	Open drain 3.3 V	-	(Optional) Used in a multiple GPU design with multiple display outputs to allow all displays in group B to update at the same time and have synchronous left/right stereo timing. In a multiple GPU design where displays are connected to more than one GPU, connect SWAPLOCKB from all GPUs together with an external 10-kΩ pull-up resistor. GPU genlock is needed, either via a genlock system or by feeding all GPUs with the same reference clock.

3.13 Display Identification Interface

Table 3–14 Display Identification Interface

Pin Name	Type	Description
DDC1CLK/ DDC1DATA **or** **AUX1P/N**	I/O	DDC1CLK/DDC1DATA and AUX1P/N signal pairs are mutually exclusive. A design can use either the DDC1 or AUX1 pair on one display connector. Alternatively, DDC1DATA can be connected to AUX1N, and DDC1CLK can be connected to AUX1P for use on one DisplayPort connector (see reference schematics). **Note:** Can be unconnected if not used. For the DDC functionality (DDC data and clock signals (I^2C master)): • These pins can be used to support internal high-bandwidth digital content protection (HDCP). • Outputs are open drain and 3.3-V tolerant only; NOT 5-V tolerant. Level shifter from 5 V to 3.3 V is required on the PCB. For the AUX functionality (auxiliary differential signals for DisplayPort): • A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector, and • A source detection pull-down resistor (100-kΩ 5% tolerance) is required on the AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on the AUXN signal.
DDC2CLK/ DDC2DATA **or** **AUX2P/N**	I/O	DDC2CLK/DDC2DATA and AUX2P/N signal pairs are mutually exclusive. A design can use either the DDC2 or AUX2 pair on one display connector. Alternatively, DDC2DATA can be connected to AUX2N, and DDC2CLK can be connected to AUX2P for use on one DisplayPort connector (see reference schematics). **Note:** Can be unconnected if not used. For the DDC functionality (DDC data and clock signals (I^2C master)): • These pins can be used to support internal HDCP functionality. • Outputs are open drain and 3.3-V tolerant only; NOT 5-V tolerant. Level shifter from 5 V to 3.3 V is required on the PCB. For the AUX functionality (auxiliary differential signals for DisplayPort): • A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector, and • A source detection pull-down resistor (100-kΩ 5% tolerance) is required on the AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on the AUXN signal.
DDCAUX[6:3]N **DDCAUX[6:3]P**	I/O	DDC data/clock for DVI/HDMI or auxiliary differential signals for DisplayPort. These pins can be used to support internal HDCP. **Note:** Can be unconnected if not used. For the AUX functionality: • A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector, and • A source detection pull-down resistor (100-kΩ 5% tolerance) is required on each AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on each AUXN signal. For the I^2C functionality: Outputs are open drain and 3.3-V tolerant; NOT 5-V tolerant. Level shifter from 5 V to 3.3 V is required on the PCB.
HPD1 **GENERICC_HPD2**	I	Hot-plug detect signal from the display device to the GPU.

Pin Name	Type	Description
GENERICD_HPD3		
GENERICE_HPD4		
GENERICF_HPD5		
GENERICG_HPD6		

3.14 Test/JTAG Interface

In order to debug issues, AMD requires access to the JTAG and debug ports unless specified otherwise.

Test points can be used on the JTAG signals to minimize the PCB space needed.

Note: The JTAG interface on "Vega 10" is 1.8 V.

Table 3–15 Test/JTAG Interface

Pin Name	Type	Description
TESTEN	I 1.8 V (VDDAN_18)	Reserved signal. This pin must be tied to ground through a 1-kΩ to 10-kΩ resistor for normal GPU operation.
TRST_L	I 1.8 V (VDDAN_18)	TRSTB (test reset). This pin can be left floating, or tied to 1.8 V through a 10-kΩ resistor for normal GPU operation. Must be accessible on all PCBs through a test point or resistor pad.
TDI	I 1.8 V (VDDAN_18)	TDI (test data input). This pin can be left floating, or tied to 1.8 V through a 10-kΩ resistor for normal GPU operation. Must be accessible on all PCBs through a test point or resistor pad.
TCK	I 1.8 V (VDDAN_18)	TCK (test clock). This pin can be left floating, or tied to ground through a 10-kΩ resistor for normal GPU operation. Must be accessible on all PCBs through a test point or resistor pad.
TMS	I 1.8 V (VDDAN_18)	TMS (test mode select). This pin can be left floating, or tied to 1.8 V through a 10-kΩ resistor for normal GPU operation. Must be accessible on all PCBs through a test point or resistor pad.
TDO	O 1.8 V (VDDAN_18)	TDO (test data output). This pin can be left floating, or unconnected if not used. Must be accessible on all PCBs through a test point or resistor pad.
DBREQ_L	I 1.8 V (VDDAN_18)	Additional debug input. This pin must have a 1 kΩ pullup to 1.8 V and a 0.01 µF filter capacitor to ground.

3.15 Debug Port

Table 3–16 Debug Port

Pin Name	Functional Name
SMBCLK	SMBus clock. Connected to the SMBCLK line of the SMBus master with an external pull-up resistor to 3.3 V. Supports the SMBus 2.0 protocol.
SMBDAT	SMBus data. Connected to the SMBDAT line of the SMBus master with an external pull-up resistor to 3.3 V. Supports the SMBus 2.0 protocol.
TEST6	Connect to ground through a 0-Ω resistor on the PCB.
BP_[0:3]	Connect to 1.8 V through pull-up resistors on the PCB.
INTCRACKMONDA	Not connected on the PCB.
INTCRACKMONDB	
INTCRACKMONGLL	
INTCRACKMONGLR	
INTCRACKMONGUL	
INTCRACKMONGUR	
INTCRACKMONP	
INTCRACKMONPDG	
XTRIG6	Provide a pull-up resistor footprint to 1.8 V on the PCB.
XTRIG7	Provide a pull-up resistor footprint to 1.8 V on the PCB.
ANALOGIO	Provide access on the PCB through a test pad.
PINSTRAP_[0:7]	Debug bus output data.
DFTIO_ [0:383]	Not connected on the PCB.
PLLCHARZ1_L **PLLCHARZ1_H**	Each of the two balls should be connected to a capacitor (0.1 µF) in series with a resistor (51.1 Ω) to ground.

3.16 Thermal Information and Management Interface

Table 3–17 Thermal Interface Signals

Pin Name	Type	Description
DPLUS	Anode	DPLUS: Thermal diode plus side (anode), used by the external temperature controller to obtain GPU die temperature.
DMINUS	Cathode	DMINUS: Thermal diode minus side (cathode), used by the external temperature controller to obtain the GPU die temperature. **Note:** Can be unconnected if not used. DPLUS and DMINUS routing must have minimum resistance; less than 0.02Ω. Routed as differential pair, referencing to ground with minimal plane crossings, and kept away from high speed signals.
TEMPIN[1]	I	TEMPIN: A provision to connect to the anode of an external thermal diode (or base and collector of NPN transistor) for the GPU to read the temperature from a spot of interest on the board or platform.

Pin Name	Type	Description
TEMPINRETURN[1]	I	TEMPINRETURN: A provision to connect to the cathode of an external thermal diode (or emitter of NPN transistor) for the GPU to read the temperature from a spot of interest on the board or platform.
PROCHOT_L	I/O	Active low. Can be configured as input to receive thermal interrupt from the external thermal sensor. Can be configured as output (open drain) to inform the system that the GPU die temperature is above a certain threshold.
FANOUT	O	Fan speed control output. Fan drive output (output to control fan). In PWM mode, the PWM frequency is 15 kHz to 50 kHz. Provide a 10-KΩ pull-down resistor to ground.
FANIN	I	Fan speed input.
CTF	O	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the graphics card or platform can protect the GPU from damage by removing power. If CTF is expected to be latched at “high” level upon occurrence of the CTF event, 1.8 V and 3.3 V to the GPU must remain. The CTF setpoint is 91°C for air cooled designs, and 76°C for liquid cooled designs.
ALERT_L	I/O	For debug purposes. Not connected on the PCB.
PUMPIN	I	Pump speed input from the liquid cooled solution. Regular 3.3 V TACH input.
PUMPOUT	O	Pump speed control output to the liquid cooled solution. Provide a 10-KΩ pull-down resistor to ground.

1. **Route the two signals differentially; kept away from high-speed switching signals.**
   Total resistance of the nets including return path should be less than 1 Ω.
   Add a filter capacitor between TEMPIN and TEMPINRETURN as close to the GPU as possible.

3.17 SMBus Interface

Table 3–18 SMBus Interface

Pin Name	Type	Description
SMBDAT	I/O	SMBus Data: Connected to the SMBDAT line of the SMBus master with an external pull-up resistor to 3.3 V.
SMBCLK	I/O	SMBus Clock: Connected to the SMBCLK line of the SMBus master with an external pull-up resistor to 3.3 V. Supports the SMBus 2.0 protocol. The SMBus slave address can be set to either 0×40 or 0×41 through pin strap on GPIO_19. For more details, see Table 3–24 (p. 38). AMD reserves SMBUS slave address 0×4C for testing purpose. Platform must not communicate with GPU, or any device on the same SMBUS as GPU, using slave address 0×4C. The GPU also supports ARP.

3.18 PLL Interface

Table 3–19 PLL Interface

Pin Name	Type	Description
XTALIN	I	Connect a 27-MHz parallel-resonant crystal between XTALIN and XTALOUT as a reference clock to the GPU. Crystal characteristics: • ESR: < 80 Ω. • Combined frequency tolerance and stability: ±30 ppm max. A 1-MΩ resistor must be connected between XTALIN and XTALOUT when a crystal is used. Capacitive loading from the package and PCB trace should be subtracted from the C1 and C2 capacitor values.
XTALOUT	O	See above.
REFCLKN **REFCLKP**	I	100 MHz differential reference clock (+/-) input for GPU PLLs, e.g.,TMDP PLL Display PLL. 200 ps (max) cycle to cycle jitter. 300 ps (max) long term jitter (10,000 cycles after the trigger edge). Non-spread. Refer to the clock specs in Table 3–20 (p. 35).
OSC_GAIN[0:2]	I/O 3.3 V (VDDAN_33)	Provide a pull-up resistor to 3.3 V and a pull-down resistor to GND for each pin on the PCB. By default, install only pull-up resistors on OSC_GAIN[2:1], and install only pull-down resistor on OSC_GAIN[0].
Note: Both the 27-MHz crystal and 100-MHz differential clock must be provided to the GPU.		

Table 3–20 External Input Clock Requirements for REFCLKN/P

Symbol	Parameter and test conditions	Min	Typ	Max	Units	Notes
Freq	Frequency		100		MHz	
V_{IH}	Differential Input High Voltage	+150			mV	Differential waveform
V_{IL}	Differential Input Differential waveform			-150	mV	Differential waveform
V_{CROSS}	Absolute crossing point voltage	+250		+550	mV	Single-ended crossing
ΔV_{CROS}	Variation of Vcross over all rising clock edges			+140	mV	
V_{swing}	Voltage Swing	-0.3	0.76	1	V	Single-Ended including overshoot/undershoot
T_{fall}/T_{rise}	Rise/Fall time	0.6		4.0	V/ns	Measured from 150-mV to 150-mV differential

3.19 AMD PowerXpress™ Interface

Table 3–21 AMD PowerXpress™ Interface

Pin Name	Type	PD/ PU	Description
PX_EN	O (VDDAN_33)	PD	On/off regulator control signal for AMD ZeroCore Power feature (BACO mode). High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal PWRGOOD is asserted and PERSTb is de-asserted. Can be left unconnected if not used.

3.20 Power and Ground Descriptions and Operating Conditions

Note:

- All power and ground pins must always be connected.

Table 3–22 Power and Ground Descriptions and Operating Conditions

Pin Name	Voltage	Description
VDDCI_MEM	0.9 V	Isolated (clean) core power for the l/O logic of HBM2PHY.
FB_VDDCI_MEM	-	Provides VDDCI_MEM feedback path to the regulator. If unused, connect to test point or leave unconnected.
VDDIO_MEM	1.35 V	I/O power for the memory interface
FB_VDDIO_MEM_GPU	-	Provides VDDIO_MEM feedback path from HBM2PHY to the regulator. If unused, connect to test point or leave unconnected.
FB_VDDIO_MEM_HBM	-	Provides VDDIO_MEM feedback path from DRAM to the regulator. If unused, connect to test point or leave unconnected.
VDDCR_HBM	1.35 V	Power for internal logic of DRAM.
FB_VDDCR_HBM	-	Provides VDDCR_HBM feedback path to the regulator. If unused, connect to test point or leave unconnected.
VPP	2.5 V	Pump voltage of DRAM.
VDDCR_BACO	0.9 V	Separate core power for the PCIe bus logic. Can be supplied by the same voltage regulator that powers VDD_080_EFUSE and VDD_080, but a bead should be used to isolate VDDCR_BACO.
VDD_080_EFUSE	0.9 V	Efuse internal supply. Can be merged with VDD_080 and supplied by the same regulator.
VDD_080	0.9 V	Supply for TMDP, PLL, PCIE, DFS, and XTAL.
VDD_18	1.8 V	1.8-V supply for TMDP, PLL, PCIE, CLKstretch, HBM2PHY, XTAL, and TMON. Must remain powered whenever VDDAN_33 is powered.
VDDAN_18	1.8 V	1.8-V supply for GPIO and AUX. Must remain powered whenever VDDAN_33 is powered. Can be merged and share the same regulator with VDD_18.

Pin Name	Voltage	Description
VDDAN_Q_EFUSE	1.8 V	Can be merged and share the same regulator with VDD_18.
VDDCR_SOC	0.8 V - 1.25 V	Dedicated core power; provides power to the internal logic. SVI2 regulator set voltage.
FB_VDDCR_SOC	-	Provides VDDCR_SOC feedback path to the regulator. If unused, connect to a test point or leave unconnected.
VDDAN_33	3.3 V	I/O power for 3.3-V pins, such as GPIOs and AUX.
VSS	0 V	Ground.
FB_VSS_A	FB of VSS	Provides VSS_A feedback path to the regulator. Route differentially with FB_VDDCR_SOC to the core regulator. If unused, connect to a test point or leave unconnected.
FB_VSS_B	FB of VSS	Provides VSS_B feedback path to the regulator. Route differentially with FB_VDDIO_MEM_HBM/ FB_VDDIO_MEM_GPU/FB_VDDCR_HBM to the memory regulator. If unused, connect to a test point or leave unconnected.

Table 3–23 Other Signals

Pin Name	Type	Description
TEST_PG **TEST_PG_BACO**	I/O (VDDAN_18)	TEST_PG and TEST_PG_BACO must be connected to the 1.8-V power rail through pull-up resistors for normal operation.
TS_A	I/O (VDD_18)	Not connected on the PCB. Provide test pad.
GENERICA/B	I/O (VDDAN_33)	General purpose I/O or open-drain output.
MACO_EN	I/O	Reserved for future purposes.

3.21 Configuration Straps

3.21.1 Pin-based Straps

"Vega 10" uses pin straps (i.e., one pin for one strap).

Some of the straps are on 3.3-V GPIOs while others are on dedicated 1.8-V strap pins.

Each strap pin has either an internal pull-down resistor which provides a default value of 0, or an internal pull-up resistor which provides a default value of 1, at power up. For each strap that defaults to 0 by the GPU, provide a pull-up resistor option (to 3.3-V or 1.8-V depending on if the pin is 3.3 V to 1.8 V) on the PCB. For each strap that defaults to 1 by the GPU, provide a pull-down resistor option to GND on the PCB.

Any external circuit using these pins must not conflict with the logic level required by the strap after power up until PCIe reset gets de-asserted.

Table 3–24 Pin-based Straps

Strap Name	Pin Name	Power Rail	Description	GPU Default	Recommended Settings[1]
BIF_VGA_DIS	GPIO_15	VDDAN_33	Determine whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space). 0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller.	0 (Internal pull-down)	0 Provide a pull-up resistor option to VDDAN_33.
ROM_CONFIG [2:0]	PINSTRAP_2 PINSTRAP_1 PINSTRAP_0	VDDAN_18	If BIOS_ROM_EN = 1, ROM_CONFIG [2:0] defines the ROM type. See ROM Configurations (p. 40) for details. If BIOS_ROM_EN = 0, then ROM_CONFIG [2:0] defines the primary memory aperture size. Not applicable to "Vega 10".	101 (Internal pull-up/ pull-down)	101 Provide a pull-down resistor option to GND on the PCB for PINSTRAP_2. Provide a pull-up resistor option **to 1.8 V** on the PCB for PINSTRAP_1. Provide a pull-down resistor option to GND on the PCB for PINSTRAP_0.
BIOS_ROM_EN	GPIO_10	VDDAN_33	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. Not applicable to "Vega 10". 1: Enable external BIOS ROM device. **Note:** When an external BIOS ROM device is used, GPIO_10 also connects to the ROM device's chip select (active low).	1 (Internal pull-up)	1 Provide a pull-down resistor option to GND on the PCB. AMD requires dedicated ROM for video BIOS be used on all "Vega 10" designs. This strap should be set to 1.
Special Usage [1] Special Usage [0]	GPIO_12 GPIO_11	VDDAN_33	Special usage	0 (Internal pull-down)	Design dependent. Refer to application note order #55739 on the special usage. Provide a pull-up resistor option to VDDAN_33 on the PCB for each pin.

Strap Name	Pin Name	Power Rail	Description	GPU Default	Recommended Settings[1]
AUD_PORT_CONN [2:0]	PINSTRAP_5 PINSTRAP_4 PINSTRAP_3	VDDAN_18	Determine the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the GPU itself, the number and type of connectors on the board (DP/HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. 111: No usable endpoints 110: One usable endpoint 101: Two usable endpoints 100: Three usable endpoints 011: Four usable endpoints 010: Five usable endpoints 001: Six usable endpoints 000: All endpoints are usable	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option **to 1.8 V** on the PCB for each pin.
CONFIG [2:0]	GPIO_18 GPIO_17 GPIO_16	VDDAN_33	Provide a pull-up resistor option to VDDAN_18 on the PCB for each pin. Provides an option to specify certain board-level specifics to the VBIOS or driver.	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option **to VDDAN_33** on the PCB for each pin.

Strap Name	Pin Name	Power Rail	Description	GPU Default	Recommended Settings[1]
SMBUS_ADDR	GPIO_19	VDDAN_33	Provide a strap option to change the SMBUS slave address of the GPU. 0: 0×41 1: 0×40	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option to VDDAN_33 on the PCB for the pin.
BIF_GEN3_DIS_A	PINSTRAP_6	VDDAN_18	Disable/Enable PCIe Gen3 capability. 0: PCIe Gen3 is supported. 1: PCIe Gen3 is not supported.	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option to 1.8 V on the PCB.
BIF_CLK_PM_EN	PINSTRAP_7	VDDAN_18	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option to 1.8 V on the PCB.
BIF_LC_TX_SWING	GPIO_13	VDDAN_33	Controls the transmitter full/ reduced swing mode. 0: The transmitter full-swing is enabled. 1: The transmitter reduced-swing is enabled.	0 (Internal pull-down)	0 Provide a pull-up resistor option to VDDAN_33 on the PCB.

3.21.2 ROM Configurations

For designs that have a dedicated ROM device for the GPU video BIOS:

- Use the GPU default strap on GPIO_10 (i.e., 1).
- Use the GPU default straps on PINSTRAP[2:0] (i.e., 101).

3.21.3 ROM Straps for Add-in Card Design

If the ROM is attached (see ROM_CONFIG[2:0] pin-based straps), after PERSTB goes inactive (high), the ROM is read at the addresses listed below and default settings are applied.

The ROM based straps are ORed with the pin-based straps.

Table 3–25 Rom-based Straps

Strap Name	Description	BIOS Address	Default BIOS Setting
STRAP_BIF_STRAP_64BAR_DIS_DEV0_F0	Enable 64-bit BAR for Function 0. Affects bit 2 of BLOCK_MEM_TYPE for each BAR register in the PCI configuration space.	0×A8 Bit 26	0
STRAP_BIF_STRAP_SUBSYS_VEN_ID_DEV0_F0	Subsystem Vendor ID (SSVID) in the PCI configuration space. If the VBIOS ROM is not used, then the SBIOS is permitted to overwrite this register for each PCI function on the device before the enumeration cycle is initiated, otherwise the default value is used.	0×B8 Bit 29 to 0×BC Bit 12	0×1002
STRAP_BIF_STRAP_SUBSYS_ID_DEV0_F0	Subsystem ID (SSID) for the PCI configuration space for Function 0. If enabled, the SSID for the secondary display function (F1) is the set to the same value as the primary display function (F0) with bit 0 inverted.	0×B0 Bits 4 to 19	
STRAP_BIF_STRAP_MEM_AP_SIZE_DEV0_F0	Size of the primary memory apertures claimed in the PCI configuration space. 000 = 256 MB 001 = 512 MB 010 = 1 GB 011 = 2 GB 100 = 4 GB 101 = 8 GB 110 = 16 GB 111 = 32 GB It is a shared pin strap with ROM_CONFIG[2:0] if BIOS_ROM_EN is set to 0.	0×C0 Bits 7 to 9	Depends on board configuration.
STRAP_BIF_STRAP_FUNC_EN_DEV0_F1	Multi-function device select. Affects bit 7 of the Header register in PCI configuration space. PCI configuration setting: 0 - Audio function not present. 1 - Audio function present. Boards with a ROM will require both the ROM and the specific pin straps to be	0×B8 Bit 12	Depends on board configuration.

Strap Name	Description	BIOS Address	Default BIOS Setting
	set in order to enable the audio function. Boards without a ROM will only require the pin straps to be set in order to enable the audio function.		
STRAP_BIF_STRAP_VGA_DIS_DEV0_F0	VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0 – VGA Controller capacity enabled. 1 – The device will not be recognized as the system’s VGA controller.	0×C0 Bit 22	0

4

Timing Specifications

This chapter describes bus and memory timing specifications of "Vega 10".

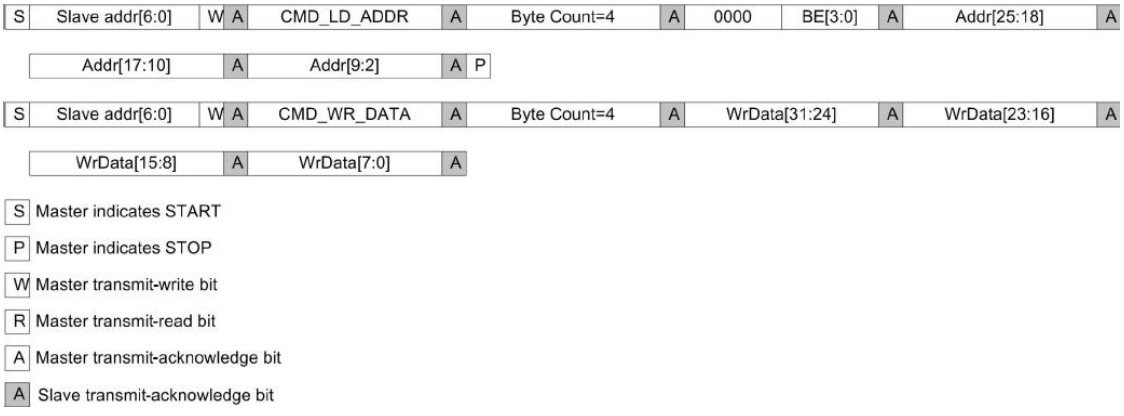
To link to a topic of interest, use the following list of linked cross-references:

4.1 SMBus Timing

4.1.1 SMBus Write Cycle

The following figure shows an SRBM (system register bus manager) write cycle on the SMBus interface.

Figure 4–1 SMBus Write Cycle



A typical SMBus write cycle consists of the following steps:

1. Issuing a Load Address Command to the SMB_ADDR register:
   a. The SMBus master issues a START bit to the slave.
   b. The SMBus master issues 7-bit slave address to the slave.
   c. The SMBus master issues a write bit to the slave.

d. The SMBus slave acknowledges the master.

e. The SMBus master issues an 8-bit CMD_LD_ADDR command to the slave.

f. The SMBus slave acknowledges the master.

g. The SMBus master sends a byte count (always 4).

h. The SMBus slave acknowledges the master.

i. The SMBus master issues a 4-bit byte enable with a 4-bit zero padding.

j. The SMBus slave acknowledges the master.

k. The SMBus master sends SMB_ADDR[25:18] to the slave.

l. The SMBus slave acknowledges the master.

m. The SMBus master sends SMB_ADDR[17:10] to the slave.

n. The SMBus slave acknowledges the master.

o. The SMBus master sends SMB_ADDR[9:2] to the slave.

p. The SMBus slave acknowledges the master.

q. The SMBus master sends a STOP bit to the slave.

2. Issuing a Write Data Command to the SMB_WR_DATA register:

a. The SMBus master issues a START bit to the slave.

b. The SMBus master issues a 7-bit slave address to the slave.

c. The SMBus master issues a write bit to the slave.

d. The SMBus slave acknowledges the master.

e. The SMBus master issues an 8-bit CMD_WR_DATA command to the slave.

f. The SMBus slave acknowledges the master.

g. The SMBus master sends a byte count (always 4).

h. The SMBus slave acknowledges the master.

i. The SMBus master sends SMB_WR_DATA[31:24] to the slave.

j. The SMBus slave acknowledges the master.

k. The SMBus master sends SMB_WR_DATA[23:16] to the slave.

l. The SMBus slave acknowledges the master.

m. The SMBus master sends SMB_WR_DATA[15:8] to the slave.

n. The SMBus slave acknowledges the master.

o. The SMBus master sends SMB_WR_DATA[7:0] to the slave.

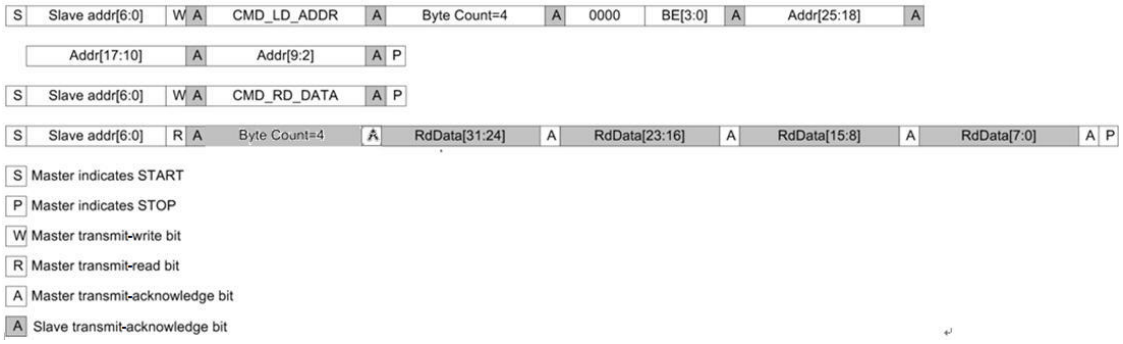
p. The SMBus slave acknowledges the master.

q. The SMBus master sends a STOP bit to the slave.

4.1.2 SMBus Read Cycle

The following figure shows an SRBM read cycle on the SMBus interface.

Figure 4–2 SMBus Read Cycle



A typical SMBus read cycle consists of the following steps:

1. Issuing a Load Address Command to the SMB_ADDR register:
   - **a.** The SMBus master issues a START bit to the slave.
   - **b.** The SMBus master issues a 7-bit slave address to the slave.
   - **c.** The SMBus master issues a write bit to the slave.
   - **d.** The SMBus slave acknowledges the master.
   - **e.** The SMBus master issues an 8-bit CMD_LD_ADDR command to the slave.
   - **f.** The SMBus slave acknowledges the master.
   - **g.** The SMBus master sends a byte count (always 4).
   - **h.** The SMBus slave acknowledges the master.
   - **i.** The SMBus master issues a 4-bit byte enable with a 4-bit zero padding. These bits should have no effect on the reads.
   - **j.** The SMBus slave acknowledges the master.
   - **k.** The SMBus master sends SMB_ADDR[25:18] to the slave.
   - **l.** The SMBus slave acknowledges the master.
   - **m.** The SMBus master sends SMB_ADDR[17:10] to the slave.
   - **n.** The SMBus slave acknowledges the master.
   - **o.** The SMBus master sends SMB_ADDR[9:2] to the slave.
   - **p.** The SMBus slave acknowledges the master.
   - **q.** The SMBus master sends a STOP bit to the slave.
2. Issuing a Read Data Command to the slave.
   - **a.** The SMBus master issues a START bit to the slave.
   - **b.** The SMBus master issues a 7-bit slave address to the slave.

c. The SMBus master issues a write bit to the slave.

d. The SMBus slave acknowledges the master.

e. The SMBus master issues an 8-bit CMD_RD_DATA command to the slave.

f. The SMBus slave acknowledges the master.

g. The SMBus master terminates the transaction with a STOP.

3. Issuing an SMBus read to the slave:

a. The SMBus master issues a START bit to the slave.

b. The SMBus master issues an 7-bit slave address to the slave.

c. The SMBus master issues a read bit to the slave.

d. The SMBus slave acknowledges the master.

e. The SMBus slave sends a byte count (always 4).

f. The SMBus master acknowledges the slave.

g. The SMBus slave sends SMB_RD_DATA[31:24] to the master.

h. The SMBus master acknowledges the slave.

i. The SMBus slave sends SMB_RD_DATA[23:16] to the master.

j. The SMBus master acknowledges the slave.

k. The SMBus slave sends SMB_RD_DATA[15:8] to the master.

l. The SMBus master acknowledges the slave.

m. The SMBus slave sends SMB_RD_DATA[7:0] to the master.

n. The SMBus master acknowledges the slave.

o. The SMBus master terminates the transaction with a STOP.

4.1.3 SMBus Read Thermal Sensor

Programming sequence is shown below:

1. SMB Issue a Load Address Command (cmd1) to the CG_MULT_THERMAL_STATUS address. (Tell SMBus slave which register to read.)

   82 01 04 0f 01 66 5A

2. SMB Issue a Read Data Command (cmd3) (Tell SMBus slave to read out thermal value.)

   82 03 83 <value read back>

3. Repeat step 2.

4.2 Initialization Sequence and Timing

4.2.1 Initialization Sequence and Timing

1. Chip reset (PERSTB) is asserted, and PCIE_REFCLK starts running.
2. All GPIOs go to a tristate (input) mode at RESETB. Some GPIOs have internal pull-down (PD) or pull-up (PU) resistors—see descriptions of pin-based straps.
3. External pin straps are driving their values onto the GPU pins.
4. Chip reset (PERSTB) is deasserted.
5. External pin-strap values are latched internally.
6. In parallel:
    a. eFuse state machine begins to read "eFuse straps."
    b. If a ROM exists (and is programmed), a request is sent to the ROM controller to read the "ROM straps."
7. eFuse and ROM straps are "forwarded" to PHY.
8. In parallel:
    a. If GPU memory repair is required, then memory repair starts.
    b. eFuse and ROM straps are "forwarded" to other blocks in the GPU.
9. Wait for memory repair to complete. De-assert a hard reset to all the blocks including BIF. Enable PCIe® PHY impedance calibration. After polling for the PHY impedance calibration, distribute the remaining fuses and poll for BIF to complete its reset sequence.
10. The GPU begins link training according to the PCIe specification.

    After link training and the reset sequence are complete, the system is ready for the first transaction, such as a configuration space request.

The following figure and table provide an outline of the "Vega 10" reset sequence.

Figure 4–3 Reset Sequence

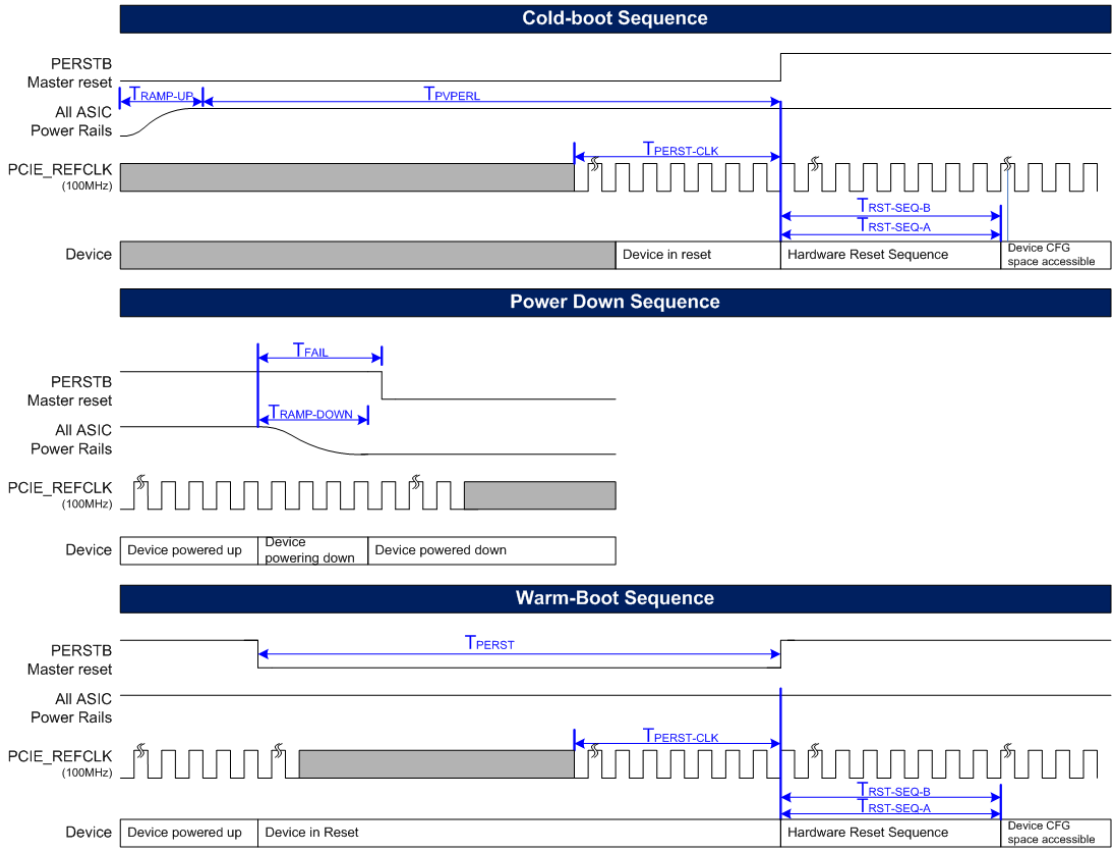


Table 4–1 Power-on Reset Sequence Timing Parameters

Parameter	Description	Minimum Time	Maximum Time
$T_{RAMP-UP}$	Power rail ramp-up time	0 ms	20 ms
T_{PVPERL}	All GPU power rails stable to PERSTB inactive	100 ms	Not limited
$T_{PERST-CLK}$	PCIE_REFCLK stable before PERSTB inactive	100 µs	Not limited
$T_{RST-SEQ-A}$	The time required by the GPU to complete its internal reset sequence, and become ready for PCI configuration space access	N/A	100 ms
$T_{RST-SEQ-B}$	The time the system software must wait after de-assertion of PERSTB before accessing the GPU's PCI configuration space	100 ms	Not limited
$T_{RAMP-DOWN}$	Power rail ramp-down time	0 ms	20 ms
T_{FAIL}	Power level invalid to PERSTB active	No requirements	No requirements
T_{PERST}	PERSTB active time	100 µs	Not limited

4.2.2 Standard Boot-up Sequence

1. PERSTB (fundamental reset) is asserted to the device.
2. Select internal-strap values are determined by the configuration of pin straps on a subset of GPIOs on the board.

3. PERSTB is deasserted, and pin-strap settings are latched permanently into the device (until PERSTB is asserted again, or the power is removed).
4. In parallel:
    a. The device begins to read "eFuse straps."
    b. If a ROM exists (and is programmed), the device begins to read "ROM straps" from its external ROM.

    Note: The system may not issue a configuration transaction to the device until the device internal reset sequence is complete.
5. For an add-in card implementation, the device completes reading the "ROM straps."
6. Device internal reset is complete. The system begins enumerating the devices attached to it by issuing configuration transactions.
7. The chip responds to any pending transaction requests, and the system continues PCI Express® enumeration, which sets up the configuration registers of the device.
8. The system copies the contents of the ROM into system memory, and executes the video BIOS, completing the device initialization. This occurs before POST begins in the system BIOS, based on the *PC 98 System Design Guide*.

    The device is ready for normal operation.

There are three configurations for strap/BIOS implementation:

Configuration 1. The controller is located on an add-in card, and there is access to a local video BIOS serial flash memory.

The ROM state machine of "Vega 10" will read in all the "ROM-based straps" right after PERSTB reset is deasserted. There are a total of 33 DWORDs of "ROM-based straps" which are stored at byte locations 0x70 through 0xF4 in the serial flash memory. See Table 3–25 (p. 41) for details.

For "Vega 10", security features have been implemented to block access to the ROM when a fuse is set. After this, when the ROM needs to be accessed, external software will have to message the SMU firmware which will authenticate the new ROM contents and write it out.

Configuration 2. The controller is located on the system motherboard and the video BIOS is stored in the system BIOS serial-flash memory (i.e., no dedicated ROM for the video BIOS).

The system BIOS will be responsible for loading the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID through an aliased address in the controller chip's configuration space. The reason for writing through an aliased address (16#4c) is that the configuration location 16#2c is read only. Any writes to this location (16#4c) will also change the content of the SUBSYSTEM_VENDOR_ID at 16#2c.

Configuration 3. A combination of configurations 1 and 2 (add-in card and device on the motherboard)

The system BIOS will take care of the graphics device on the motherboard as in case 2, while the chip on the add-in board will be taken care of as in case 1. This should cover the situation where the OS does not read the add-in card’s video BIOS because the ROM state machine from the graphics chip reads the "ROM-based straps" independently from the video BIOS.

Note: If neither the system BIOS nor the add-in card video BIOS supply the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID, their values default to the DEVICE_ID and VENDOR_ID respectively inside the chip.

4.3 Serial Flash Read/Write Timing

Figure 4–4 Serial Flash Write/Read Timing

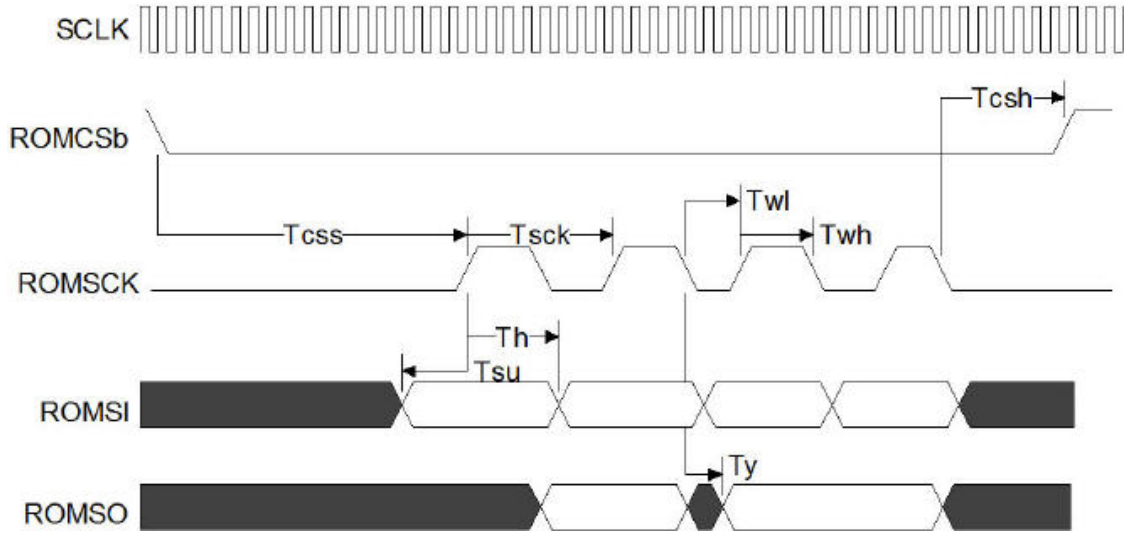
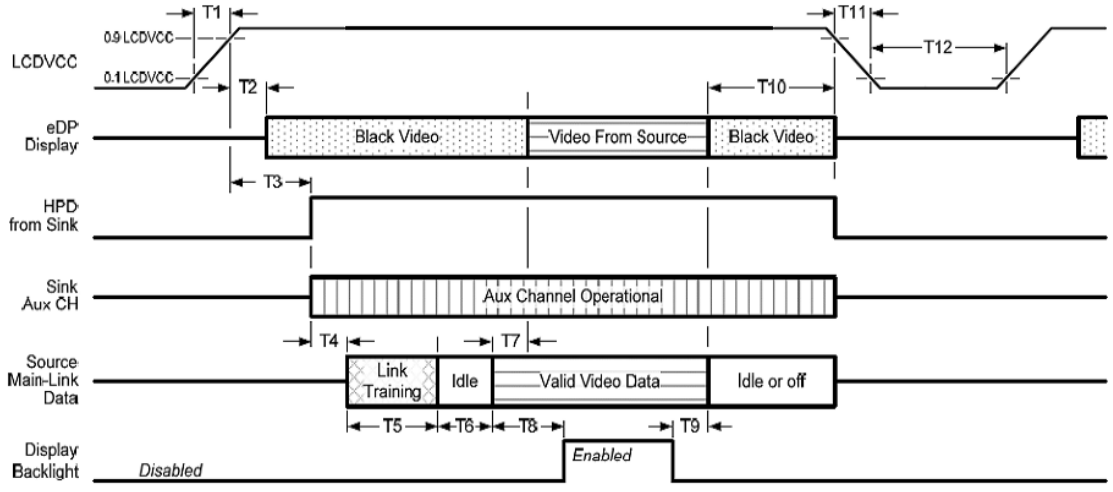


Table 4–2 Serial Flash Write/Read Timing Parameters for the Bootup Case

Symbol	Description	Min (ns)	Max (ns)
Tcss	ROMCSb falling edge to first clock sent to the device.	110	
Tsck	ROMSCK period.	70	
Twl	ROMSCK low time.	30	
Twh	ROMSCK high time.	30	
Tsu	ROMSI data setup.	20	
Th	ROMSI data hold.	40	
Ty	ROMSO data valid.	0	20
Tcsh	Last clock sent to the ROMCSb rising edge.	70	
SCLK = 100 MHz, XTALIN = 27 MHz, ROM_CNTL.SCK_PRESCALE_CRYSTAL_CLK=0x1			

4.4 LCD Panel Power-up/down Timing (eDP Interface)

Figure 4–5 eDP Panel Power-up/down Timing



Note: The Aux CH response from sink is dependent on the application of LCDVCC.

Table 4–3 Registers for Setting Backlight PWM Parameters

Parameter	Description	Time (ms)
T1+T2	Power rail rise time from 10% to 90% and delay from LCDVDCC to black video generation	Hardware controlled, up to 210 ms
T3	Delay from LCDVCC active to HPD high and Aux	Software controlled
T4	Delay from HPD high to link training initialization	Software controlled
T8	Delay from “Valid Video Data” to ENA_BL/VARY_BL active	Software controlled
T9	Delay from ENA_BL/VARY_BL inactive to the end of “Valid Video Data”	Software controlled
T10	Delay from “Source Main-Link Data” off to LCDVCC Off	Software controlled
T11	Power rail fall time from 90% to 10%	Hardware controlled, up to 10 ms
T12	Minimum panel off duration (off time is ≥ T12)	Software controlled

4.5 LCD Panel Backlight Control with PWM

Figure 4–6 Backlight PWM Parameters

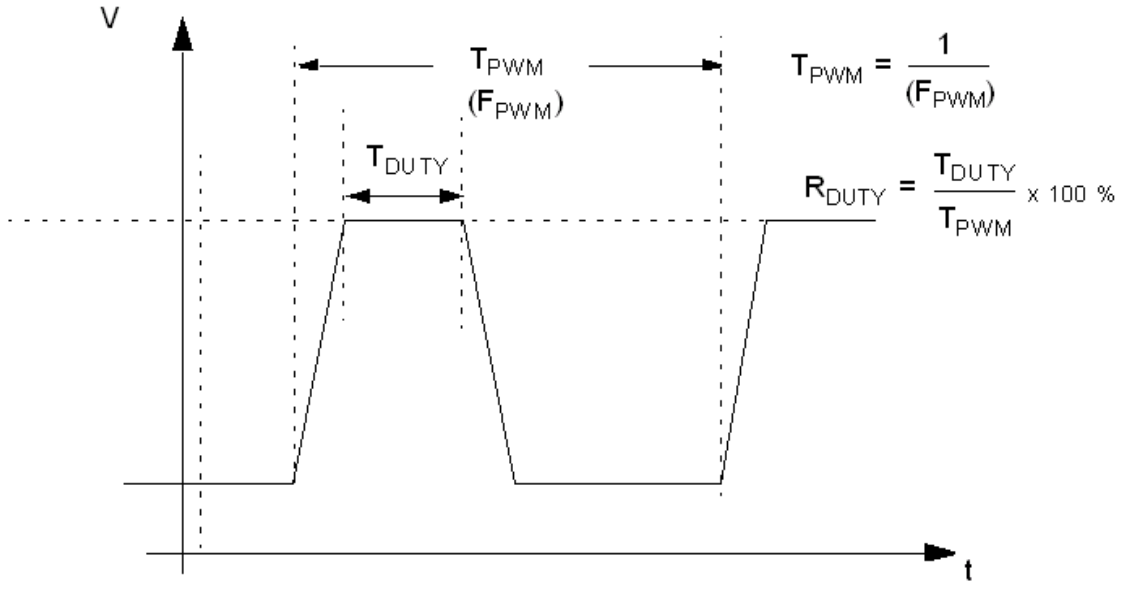


Table 4–4 Registers for Setting Backlight PWM Parameters

Register Field	Description
DISPOUT.LVTMA_PWRSEQ_REF_DIV.BL_PWM_REF_DIV	PWM frequency coarse control. This 16-bit value specifies the input reference clock divider. The frequency of the input reference clock (REF) is divided down by this amount specified. This value represents a divider of 1 to 65536. “0” is a special value that represents a divider of 65536. Other values (1 to 65535) map directly to the same divider value.
DISPOUT.BL_PWM_CNTL.BL_PWM_EN	Set to 1 to enable the PWM signal generator.
DISPOUT.BL_PWM_CNTL.BL_PWM_FRACTIONAL_EN	Set to 1 to enable fractional active duty-cycle mode. When enabled, the active duty cycle of each backlight period can vary over time to achieve the requested active duty cycle (both integer and fractional components) specified by the BL_ACTIVE_INT_FRAC_CNT value.
DISPOUT.BL_PWM_PERIOD_CNTL.BL_PWM_PERIOD_BITCNT	This 4-bit value has a dual purpose. First, it specifies the number of LSBs of the BL_PWM_PERIOD register used to represent the backlight period. The second purpose of this register is to specify how many MSBs of the BL_ACTIVE_INT_FRAC_CNT register field represent the integer component of the active duty cycle. The remaining LSBs of this register field represent the fractional component of the active duty cycle. For this register field, “0” is a special value that implies 16 bits are to be used for the period (and integer active duty cycle). Other values of 1 to 15 for this field directly map to the same number of bits to be used for the period (and MSBs of the active duty cycle as the integer component of the active duty-cycle value). When fractional active duty-cycle mode is enabled, this value should be programmed to the value that represents the smallest number of bits possible to represent the required backlight period.
DISPOUT.BL_PWM_PERIOD_CNTL.BL_PWM_PERIOD	PWM frequency fine control. Specifies the period of the backlight PWM signal. This 16-bit value represents the number of divided down input reference clock (REF /

Register Field	Description
	[BL_PWM_REF_DIV]) cycles in each backlight period. The BL_PWM_PERIOD_BITCNT register field represents how many LSBs of this register field, from 1 to 16, are actually used as the backlight period value.
DISPOUT.BL_PWM_CNTL.BL_ACTIVE_INT_FRAC_CNT	This 16-bit value specifies the backlight active duty cycle, in units of divided reference clock cycles (similar to the backlight period). This value consists of both an integer component and potentially a fractional component of the active duty cycle. The BL_PWM_PERIOD_BITCNT MSBs of this register field represent the integer component of the active duty cycle. This applies regardless of whether fractional active duty mode (BL_PWM_FRACTIONAL_EN) is enabled or disabled. The valid range for the integer component of the active duty cycle, contained in the (BL_PWM_PERIOD_BITCNT) MSBs of this register, is from 0 up to the BL_PWM_PERIOD value (contained in the (BL_PWM_PERIOD_BITCNT) LSBs of the BL_PWM_PERIOD register value). When fractional active duty cycle mode is enabled, the (16 - BL_PWM_PERIOD_CNT) LSBs of this register field represent the fractional component of the active duty cycle.

Table 4–5 Backlight PWM Parameters

Parameter	Description	Min	Typ	Max	Unit
REF	xtal_freq or xtal_freq × 2	—	27 or 54	—	MHz
F_{PWM}	Backlight PWM signal frequency. `= REF / ( [ (BL_PWM_PERIOD) × (BL_PWM_REF_DIV) ] )` where `REF` is the input reference clock frequency (typically 27 or 54 MHz), `BL_PWM_REF_DIV` is a 16-bit value specifying the division factor for this input reference clock, and `BL_PWM_PERIOD` is a 16-bit value representing the period of the backlight PWM signal in units of divided input reference clock cycles. Typical Range: 55 Hz to 50 kHz.	0.007	—	13 M	Hz
R_{DUTY}	Active duty cycle ratio. `= (BL_ACTIVE_INT_FRAC_CNT) / (BL_PWM_PERIOD)` Minimum duty cycle increment size is (1/65535) of BL_PWM_PERIOD.	0	—	100	%

The backlight pulse width modulation circuit generates a backlight PWM signal with a frequency:

```
= REFCLK / ( [ (BL_PWM_PERIOD) * (BL_PWM_REF_DIV) ] )
```

`REFCLK` is the input reference clock frequency (typically 27 or 54 MHz).

`BL_PWM_REF_DIV` is a 16-bit value specifying the division factor for this input reference clock.

`BL_PWM_PERIOD` is a 16-bit value representing the period of the backlight PWM signal in units of divided input reference clock cycles.

To set the backlight modulation,

1. Set the coarse frequency by selecting BL_PWM_REF_DIV:

   ```
   BL_PWM_REF_DIV = ceil (REF / (65535 ×
                            FTARGET))
   ```

2. Compute the fine frequency by selecting the period BL_PWM_PERIOD:

   ```
   BL_PWM_PERIOD = ceil (REF / (FTARGET ×
                            BL_PWM_REF_DIV))
   ```

   The period should be a value between 1 and 65535.

3. Compute the actual frequency:

   ```
   FINIT = REF / ((BL_PWM_PERIOD) ×
                            (BL_PWM_REF_DIV))
   ```

4. Compute the relative error:

   ```
   EINIT = (FTARGET – FINIT) / FTARGET
   ```

   Note:
   - For 50-kHz FTARGET, EINIT will equal zero (no error).
   - For 55-Hz FTARGET, EINIT will be less than 0.0006%.
   - The number of usable steps for the active duty cycle is (BL_PWM_PERIOD + 1), that is from 0% up to 100% active duty cycle.

5

Electrical Characteristics

This chapter describes the electrical characteristics of "Vega 10".

All voltages are with respect to VSS unless specified otherwise.

To link to a topic of interest, use the following list of linked cross-references:

5.1 Maximum Voltage

Note: In the below table, the VDDCR_SOC voltage and VDDCR_HBM/VDDIO_MEM voltage are defined as the command voltage sent by the GPU to the SVI2 voltage regulator through SVD data packets. The voltage for other power rails is defined at the respective power balls of the GPU. Any stress voltage greater than the absolute maximum in the table may cause permanent dmage to the device, or adversely affect the device reliability.

Table 5–1 Maximum Voltage

Supply	Maximum Voltage
VDDCR_SOC	1.25 V
VDDCI_MEM	0.954 V
VDDAN_33	3.630 V
VDDCR_HBM	1.38 V
VDDIO_MEM	
VDD_08	0.945 V
VDDCR_BACO	
VDD_080_EFUSE	
VPP	2.75 V
VDD_18	1.980 V
VDDAN_18	
VDDAN_Q_EFUSE	

5.2 Electrical Design Power

The following table lists the Thermal Design Current (TDC) numbers for all GPU power rails. Designers must ensure that their regulator circuits are capable of supplying continuous TDC safely. The regulator circuits must also meet AMD's Electrical Design Current (EDC) requirement that is defined as the minimum current for which the voltage regulator must be capable of safely supplying for a minimum of 1 ms. This means that if a voltage regulator design can safely supply this amount of current for more than 1 ms, it meets AMD's EDC criterion. EDC can be estimated tobe 1.5 times of TDC unless otherwise specified.

It is required that AMD's SVI2-compliant voltage controllers be used on all "Vega 10" designs for VDDCR_SOC. A SVI2-compliant voltage controller has two independent voltage domains built in such that one controller can deliver two power rails to the GPU (the main domain powers VDDCR_SOC, and the second domain powers VDDIO_MEM and VDDCR_HBM that are merged on the PCB), saving both cost and space compared to two-regulator solutions. Both voltage outputs are controlled through the high-speed SVI2 bus from dedicated GPU pins.

On "Vega 10"", the boot voltage of the SVI2 regulator is fixed at 0.9 V by default for both domains controlled by the GPU. Overwriting of the SVI2 boot-VID on the PCB is not allowed. 0.9 V may not be sufficient for HBM to power up properly if the second domain of the SVI2 regulator powers VDDIO_MEM/VDDCR_HBM rails. Contact AMD for guidance on setting the second domain voltage to meet HBM power up requirements.

All voltage regulators that are compliant with AMD's SVI2 specification use the SVT pin to serially stream real-time voltage and current telemetry to the GPU. "Vega 10" uses the telemetry information to enable power management features. In order to maintain the accuracy of the current measurement, it is required that the passive current-sensing components have a tolerance less than or equal to ±5%. For example, if an inductor DCR (direct current resistance) is being used as the current-sensing element, the tolerance of the DCR must be less than or equal to ±5%. Full-scale current calibration is also required. Please refer to AMD's application note, order# 54265, for details on the calibration procedure.

For the power-up sequence requirements affected by the adoption of SVI2-compliant voltage regulators, refer to Power-up/down Sequence (p. 61).

To allow for driver optimizations, faster CPUs, and new applications, designers need to provide adequate electrical margins.

The numbers are preliminary estimates and subject to change.

Table 5–2 Regulator Guidelines

Rail Name	Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDDCR_SOC	0.80 V to 1.25 V	VID_VDDC ±1.25% - I_VDDC × 0.25 mΩ	See Section Transient Behavior	300 A (TDC) 760 A (EDC)	1, 2, 4, 9, 10
VDDCR_HBM VDDIO_MEM	1.35 V	±3%	±3%	20 A (TDC) 35 A (EDC)	3
VDDCI_MEM	0.90 V	±3%	±3%	5 A (TDC)	
VDD_080 VDDCR_BACO VDD_080_EFUSE	0.90 V	±3%	±3%	5 A (TDC)	8

Rail Name	Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDD_18 VDDAN_18 VDDAN_Q_EFUSE	1.8 V	±3%	±3%	3.5 A (TDC)	5, 6, 7
VDDAN_33	3.3 V	±3%	±3%	0.1 A (TDC)	
VPP	2.5 V	±3%	±3%	1.5 A (TDC)	

Note:

1. Use the main domain of SVI2 regulator. The SVI2 regulator can provide any voltage required on VDDCR_SOC. Voltage quoted corresponds to the VID code sent from GPU to the voltage regulator in the SVD data package.
2. Sufficient EDC capacity should be allocated to the VDDCR_SOC rail in order for the GPU to burst into higher performance levels opportunistically without violating the given thermal constraints (TDC/TGP).
3. The two rails can be merged on the PCB and supplied by the second domain of the SVI2 regulator. Contact AMD for guidance on how to set the second domain of the SVI2 regulator to meet HBM power up requirements.
4. AMD requires the use of load line on the VDDCR_SOC rail. The load line value is 0.25 mΩ.
5. If a switching regulator is used to power the 1.8-V rails, a filter inductor should be placed between the output of the regulator circuit and the GPU decoupling capacitors, and outside the feedback loop of the switching regulator. The filter inductor should be of 0.24 µH, and its DCR should be of 15 mΩ or less. The LDO solution does not need the filter inductor.
6. For the switching regulator, tolerance is defined at the 1.8-V regulator output before the filter inductor.
7. The three rails can be merged on the PCB and supplied by the same regulator.
8. The three rails can be supplied by the same regulator. VDDCR_BACO should be isolated from the other two rails by a bead.
9. The quoted EDC value corresponds to the unconstrained GPU peak demand projected to cover the entire GPU population at the maximum allowed GPU die temperature and operating frequencies using a power virus-like, AMD proprietary utility that induces the heaviest transient load to GPU.
10. AMD's Peak Current Control (PCC) technology can mitigate and contain the peak demand from GPU thus reduce the EDC requirement if the required circuit is implemented on the board/platform.

5.2.1 Transient Behavior

The voltage regulator supplying VDDCR_SOC rail must exhibit equal or better transient behavior with regard to the parameters (overshoot, undershoot and settling time) listed in the following tables.

Figure 5–1 Load Insertion Legend

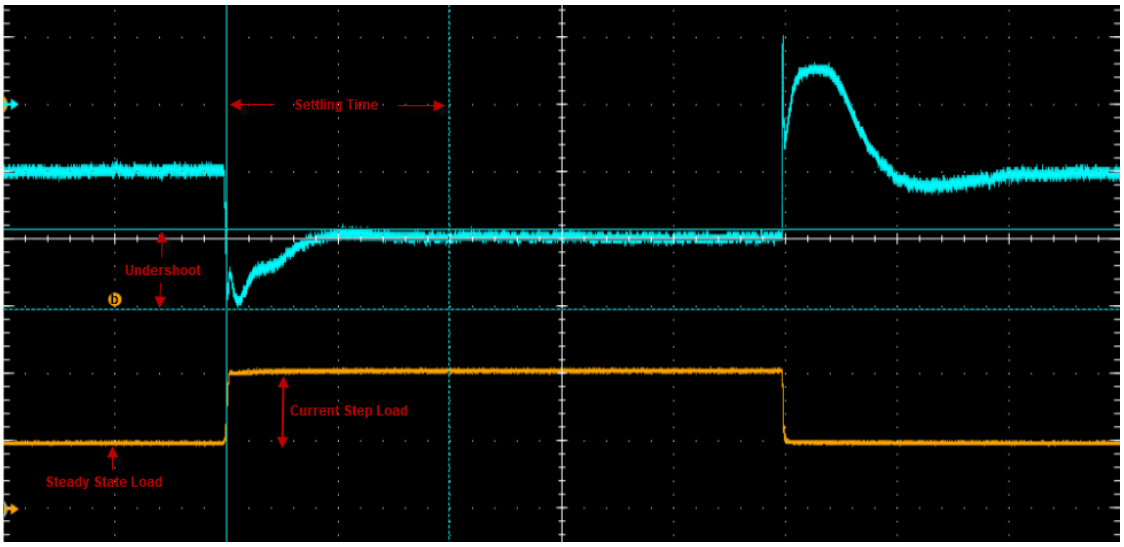


Table 5–3 Load Insertion Behavior

Current Step Load (A)	di/dt (A/us)	Max Undershoot (mV)	Max Settling Time (us)
320[1]	1037	60	20

Note: If using AMD provided SDLE for the transient study:
1. Step load is applied in addition to a 300 A steady state load.

Figure 5–2 Load Release Legend

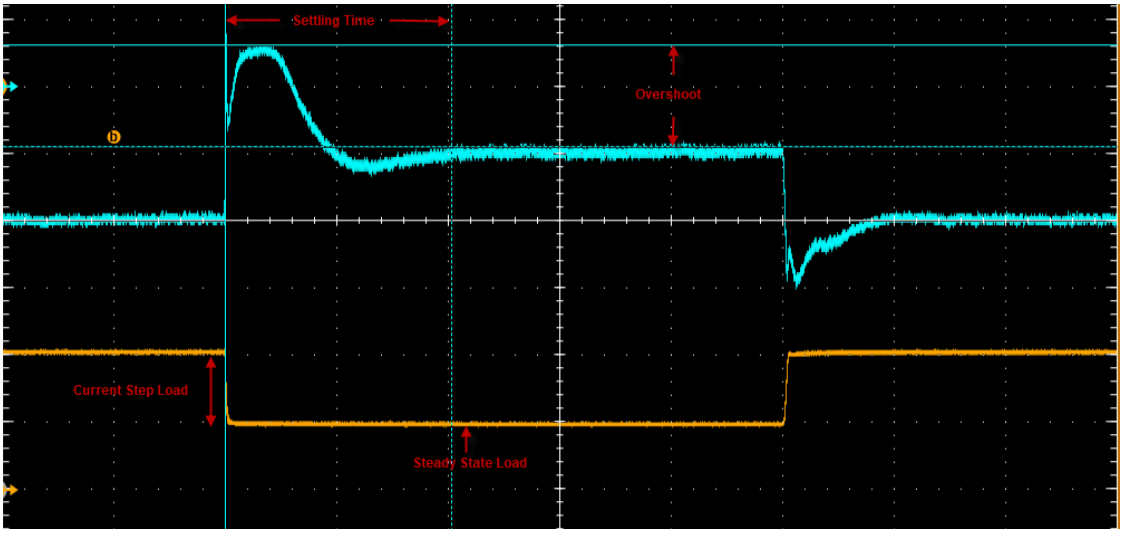


Table 5–4 Load Release Behavior

Current Step Load (A)	di/dt (A/us)	Max Overshoot (mV)	Max Settling Time (us)
320[1]	-3656	76	21

Note: If using AMD provided SDLE for the transient study:
1. Step load is applied in addition to a 300 A steady state load.

5.3 Power-up/down Sequence

"Vega 10" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDDAN_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8-V rail must reach its steady state at least 10 µs before VDDCR_SOC, VDDCR_HBM/VDDIO_MEM, VDDCI_MEM, and VDD_080/VDDCR_BACO/ VDD_080_EFUSE start to ramp up.
- VPP should reach its ready state before VDDCR_HBM/VDDIO_MEM start to ramp.

5.4 TTL Interface Electrical Characteristics

The following table provides the electrical characteristics of the TTL Interface (GPIOs).

Table 5–5 DC Characteristics for 3.3-V GPIO Pads

Parameter	Condition	Min	Max	Unit	Notes
V_{IL}—input voltage low level.	Maximum DC voltage at the PAD pin that will produce a logic low.	—	0.7	V	—
V_{IH}—input voltage high level.	Minimum DC voltage at the PAD pin that will produce logic high.	1.7	—	V	—
V_{OL}—output voltage low level.	Maximum output low voltage @ I = 8 mA.	—	0.42	V	1, 2
V_{OH}—output voltage high level.	Minimum output high voltage @ I = 8 mA.	2.5	—	V	1, 2
I_{OL}—output current low level.	Minimum output low current @ V = 0.1 V.	1.9	—	mA	1, 2
I_{OH}—output current high level.	Minimum output high current @ V = VDDR - 0.1 V.	1.9	—	mA	1, 2

5.5 DDC I^2C Mode Electrical Characteristics

The following tables provide the electrical characteristics for the DDC pins in I^2C mode.

Table 5–6 Transmitter Electrical Specification for DDC I²C

Symbol	Description	Min	Max	Unit	Notes
I2C_Tx$_{Freq}$	Supported transmittable data rate.	—	400	kHz	-
I2C_V$_{OL}$	Maximum output low voltage @ I = 8 mA.	—	300	mV	1, 2, 3
I2C_V$_{OH}$	Minimum output high voltage.	VDD5 - 0.25	—	mV	1, 2, 3, 4

Note:
1. **For detailed current/voltage characteristics, refer to the IBIS model.**
2. **Measurement taken with NMOS strength set to default values, PVT = Noml case.**
3. **The I²C interface is an open-drain circuit and pull high is determined by external power.**
4. **VDD5 refers to a 5-V external pull up.**

Table 5–7 Receiver Electrical Specification for DDC I²C Pins

Symbol	Description	Min	Max	Unit	Notes
I2C_Y_V$_{IH-AC}$	Minimum AC voltage at the PAD pin that will produce a stable high at the I2C_Y pin of the macro.	2.3		V	3
I2C_Y_V$_{IL-AC}$	Maximum AC voltage at the PAD pin that will produce a stable low at the I2C_Y pin of the macro.		1.5	V	3
I2C_Y_V$_{IH-DC}$	Minimum DC voltage at the PAD pin that will produce a stable high at the I2C_Y pin of the macro.	2.3		V	1
I2C_Y_V$_{IL-DC}$	Maximum DC voltage at the PAD pin that will produce a stable low at the I2C_Y pin of the macro.		1.5	V	1
I2C_Y_Rx$_{Freq}$	Supported received frequency.		400	kHz	-
I2C_Y$_{dc}$	I2C_Y output duty cycle.	40	60	%	2

Note:
1. **Measured with an edge rate of 1 µs at the PAD pin.**
2. **Assuming perfect duty cycle on input.**
3. **Measured at the maximum operating frequency.**

5.6 DisplayPort AUX Electrical Specification

This table provides the electrical characteristics of the DisplayPort AUX.

Table 5–8 DisplayPort AUX Electrical Specification

Symbol	Description	Min	Max	Unit	Notes
AUX_V$_{cm}$	Input/output common-mode voltage.	550	620	mV	-
AUX_V$_{diff}$	Pad differential-output swing.	525	622	mV	-
AUX_Tx$_{Freq}$	Supported transmit-data rate.	—	5	MHz	-
AUX_Rx$_{Freq}$	Supported received frequency.	—	5	MHz	-
AUX_Pad$_{dc}$	PADP/N output duty cycle.	40	60	%	1

Note:
1. **Assuming perfect duty cycle on input.**

5.7 DisplayPort Main Link Electrical Characteristics

This table provides the electrical characteristics of the DisplayPort main link.

Table 5–9 DisplayPort Main Link Electrical Specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
UI_{HIGH_RATE}	Unit interval for the DP high bit rate (2.7 Gbps/lane).	—	370	—	ps	High limit = +300 ppm Low limit = -5300 ppm
UI_{LOW_RATE}	Unit interval for the DP reduced bit rate (1.62 Gbps/ lane).	—	617	—	ps	High limit = +300 ppm Low limit = -5300 ppm
UI_{HIGH_RATE2}	Unit interval for DP high-bit rate 2 (5.4 Gbps/lane).	—	185	—	ps	High limit = +300 ppm Low limit = -5300 ppm
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$	Ratio of output voltage level 1/ level 0.	0.8		6.0	dB	-
	Ratio of output voltage level 2/ level 1.	0.1		5.1	dB	-
$V_{TX\text{-}OUTPUT\text{-}RATIO\_HBR2}$	Ratio of output voltage level 2/ level 0.	5.2		6.9	dB	-
	Ratio of output voltage level 2/ level 1.	1.6		3.5	dB	-
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$	Delta of pre-emphasis level 1 versus level 0.	2.0			dB	-
	Delta of pre-emphasis level 2 versus level 1.	1.6			dB	-
$V_{TX\text{-}PREEMP\text{-}OFF}$	Maximum pre-emphasis when disabled.			0.25	dB	-

5.8 SMBus Electrical Characteristics

The following tables provide the electrical characteristics for the SMBus DATA, CLOCK, and CLK_REQB pads.

Table 5–10 Transmitter Electrical Specification

Symbol	Description	Min	Max	Unit
F_{TX}	Supported transmit data rate.	—	100	kHz
V_{OL}	Maximum output low voltage @ I = 4 mA.	—	400	mV
V_{OH}	Minimum output high voltage.	VDD33 - 0.4	—	mV

Table 5–11 Receiver Electrical Specification

Symbol	Description	Min	Max	Unit	Notes
VIH_{AC}	Minimum AC voltage at the PAD pin that will produce a stable high at the Y pin of the macro at FRX.	2.0	—	V	3
VIL_{AC}	Maximum AC voltage at the PAD pin that will produce a stable low at the Y pin of the macro.	—	0.8	V	3
VIH_{DC}	Minimum DC voltage at the PAD pin that will produce a stable high at the Y pin of the macro.	2.0	—	V	1

Symbol	Description	Min	Max	Unit	Notes
VIL_{DC}	Maximum DC voltage at the PAD pin that will produce a stable low at the Y pin of the macro.	—	0.8	V	1
F_{RX}	Supported received frequency.	—	100	kHz	-
Y_{dc}	Y output duty cycle.	40	60	%	2
Y_{tiPDr}	Receiver propagation delay rise.	—	400	ns	1, 2, 4
Y_{tiPDf}	Receiver propagation delay fall.	—	20	ns	1, 2, 4

1. **Measured with an edge rate of 1 µs at the PAD pin.**
2. **Assuming perfect duty cycle on input.**
3. **Measured at the maximum operating frequency.**
4. **Typical simulation corner only.**

6

Thermal Data

To link to a topic of interest, use the following list of linked cross-references:

6.1 Thermal Models

For simplified thermal simulations, the Delphi model can be utilized. The compact thermal model of the ASIC is provided in the following table.

Table 6–1 ASIC Compact Thermal Model

Variable	Value
θ_{JC}: Junction to case thermal resistance (based on the two-resistor model). **Note:** Case here means the center of the top of the GPU package.	0.02°C/W
θ_{JB}: Junction to board thermal resistance (based on the two-resistor model).	2.81°C/W

6.2 Thermal Characteristics

Table 6–2 Thermal Characteristics

Variable	Value
$T_{j,op}$: Maximum recommended operating temperature. **This is the maximum temperature at which the functionality is qualified and tested. Operation above this temperature will negatively impact product reliability.** **This temperature is measured using an on-die temperature sensor near the integrated thermal diode (see Thermal Diode Characteristics (p. 66)).**	85°C (air cooled) 70°C (liquid cooled)
$T_{j,max}$: Absolute maximum rated junction temperature. **This is the maximum allowable instantaneous GPU temperature, above which damage to the GPU is likely.** **This temperature is measured using an on-die temperature sensor near the integrated thermal diode (see Thermal Diode Characteristics (p. 66)).**	91°C (air cooled) 76°C (liquid cooled)
Minimum ambient operating temperature.	0°C

6.3 Thermal Design Power

The thermal design power is defined as the power dissipated by the GPU and HBM while running a selected application at up to the maximum recommended operating temperature, and is measured as the maximum average power in a five-second moving window.

The thermal design power is intended as a recommended thermal design point; it is not an absolute maximum power under all conditions.

"Vega 10" has up to eight defined Dynamic Power Management (DPM) states, from DPM_0 to DPM_7, in ascending order of performance and power. When a graphics-demanding application (such as a game) is running, AMD's PowerTune constantly switches GPU among the states based on run-time analysis of GPU activities, power and thermal conditions. The effective power/performance depends on the percentage of time spent in each state.

The data are targets only, and are subject to change.

Table 6–3 TGP for Discrete Variants

Variant	**"Vega 10 - XTX"**		
VDDCR_SOC (V)	0.80 - 1.25		
VDDCI_MEM (V)	0.90		
VDDCR_HBM/VDDIO_MEM (V)	1.35		
DPM Level	GFXCLK (MHz)	SOCCLK (MHz)	UCLK (HBM) (MHz)
DPM_7	1600	1107	945
DPM_6	1528	1107	945
DPM_5	1440	1107	945
DPM_4	1348	1028	945
DPM_3	1269	960	945
DPM_2	1138	847	800
DPM_1	991	720	500
DPM_0	852	600	500
Memory Interface (bits)	2048		
GPU Leakage	Variable		
GPU Die Temperature (℃)	85 (air cooled) 70 (liquid cooled)		
Driver	17.20		
Test Platform	Intel Core™ i7-4790X Extreme Edition 3.6-GHz CPU, 16-GB RAM		
PCIe® Configuration	PCIe revision 3.0, up to 8.0 GT/s		
TGP Targets (W)[1]	220 (air cooled) 300 (liquid cooled)		

Note:
1. **Total consumption by GPU and HBM memory.**

6.4 Thermal Diode Characteristics

For "Vega 10", the ideality factor of the on-die thermal diode varies significantly with temperature and sourcing current. If a design chooses to use the GPU's on-die

thermal diode coupled with an external thermal sensor chip to read the GPU temperature, the external thermal sensor chip must support and enable beta compensation.

6.5 Storage Requirements

Ambient temperature: -40°C to 70°C

Relative humidity: 0% to 90%

7

Mechanical Data

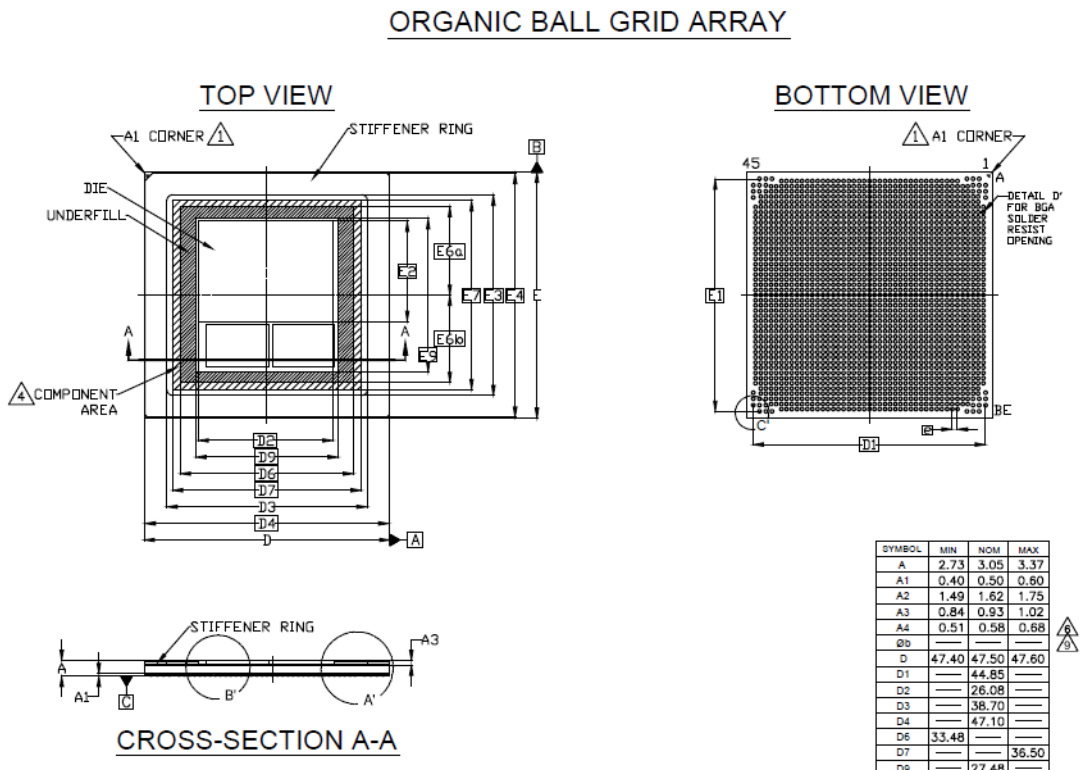
This chapter contains information on the mechanical data for "Vega 10". To go to a topic of interest, use the following list of linked cross-references:

7.1 Physical Dimensions

7.1.1 "Vega 10" Physical Dimensions

HFCBGA 47.5 mm × 47.5 mm—2013 pins

Figure 7–1 "Vega 10" Package Outline (Preliminary—MOD—00370 REV 01)



SYMBOL	MIN	NOM	MAX
A	2.73	3.05	3.37
A1	0.40	0.50	0.60
A2	1.49	1.62	1.75
A3	0.84	0.93	1.02
A4	0.51	0.58	0.68
Øb	—	—	—
D	47.40	47.50	47.60
D1	—	44.85	—
D2	—	26.08	—
D3	—	38.70	—
D4	—	47.10	—
D6	33.48	—	—
D7	—	—	36.50
D9	—	27.48	—
E	47.40	47.50	47.60
E1	—	44.85	—
E2	—	19.36	—
E3	—	38.70	—
E4	—	47.10	—
E6a	17.13	—	—
E6b	16.83	—	—
E7	—	—	36.50
E8		4.20	
E9	—	29.66	—
e		1.00	
ddd	—	—	0.305
N		2013	

NOTES :

1. THIS CORNER CONSISTS OF A TRIANGLE ON EACH SIDE OF THE PACKAGE, WHICH IDENTIFIES PIN A1 CORNER AND CAN BE USED FOR HANDLING AND ORIENTATION PURPOSES.
2. SYMBOL "N" DETERMINES NUMBER OF BALLS.
3. THIS IS A MULTI PITCH PACKAGE.
4. COMPONENTS ARE LOCATED IN THIS AREA ON PACKAGE.
5. SMT COMPONENT HEIGHT IS 0.648 MAX.
6. TOTAL THICKNESS OF STIFFENER RING AND ADHESIVE.
7. MEMORY SIZE IS 11.845~12.00 X 7.725~8.00.
8. STIFFENER RING SHOULD BE WITHIN SUBSTRATE AREA.
9. BEFORE SOLDER BALL ATTACH REFLOW, THE SOLDER BALL DIAMETER IS 0.65 NOMINAL. AFTER SOLDER BALL ATTACH REFLOW, THE SOLDER BALL DIAMETER b IS 0.68±0.12.

Figure 7–2 "Vega 10" Package Outline (Preliminary—MOD—00370 REV 01) Top View

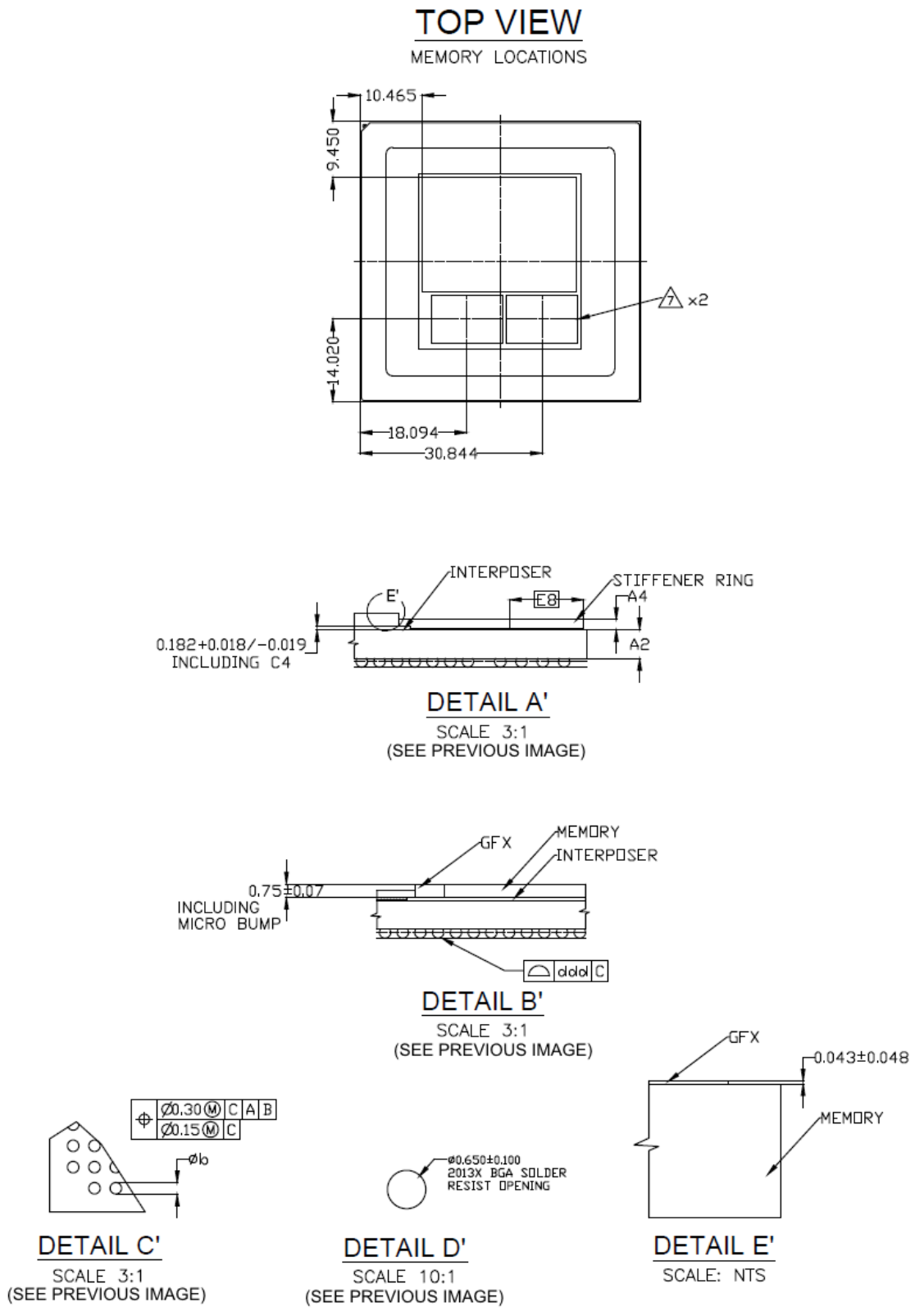
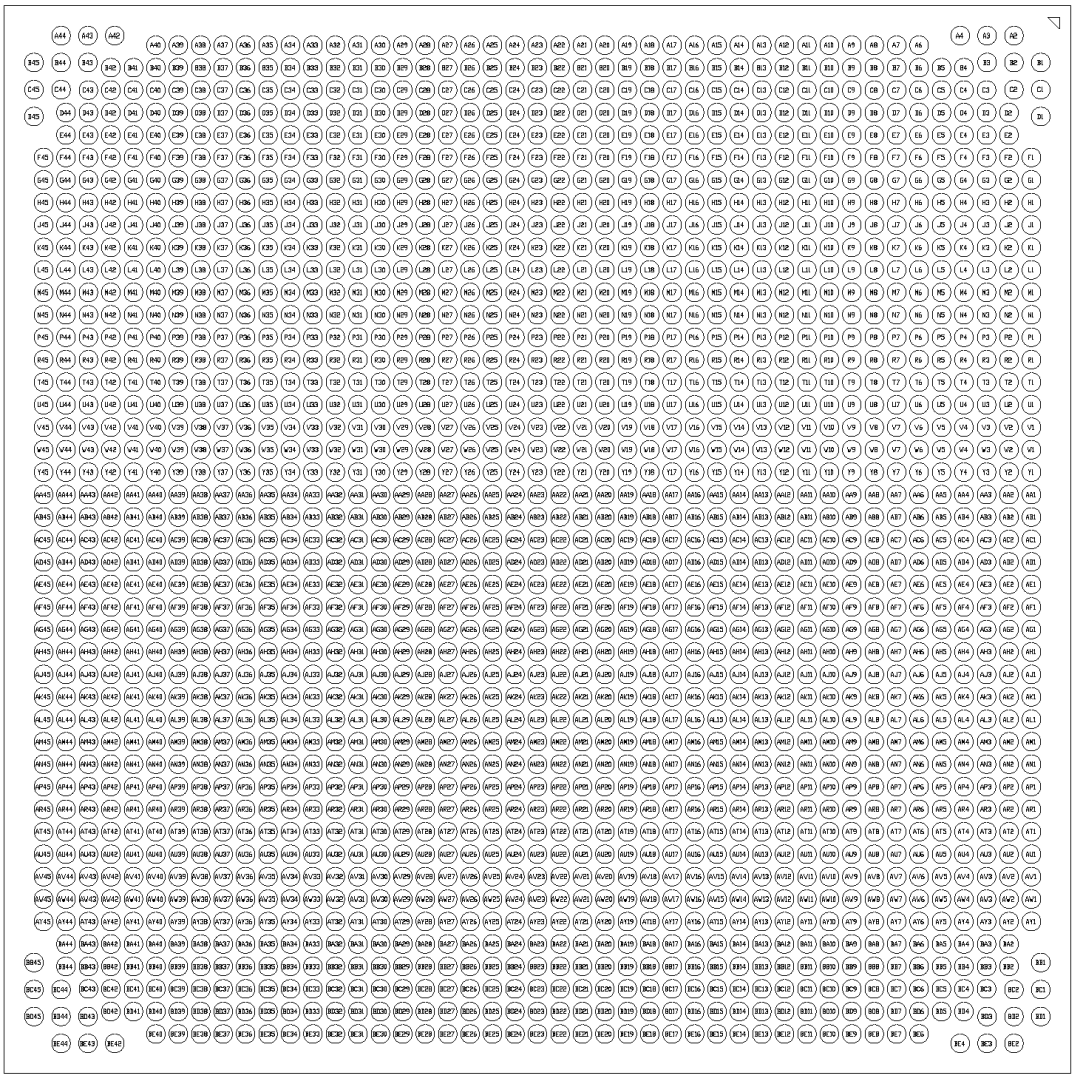


Figure 7–3 "Vega 10" Ball Names (Bottom View)



7.2 Pressure Specification

To avoid damage to the GPU (die or solder-ball joint cracks) caused by improper mechanical assembly of the cooling device, follow the following recommendations:

- It is recommended that the maximum pressure that is evenly applied across the contact area between the thermal management device and the die does not exceed 75 PSI. A contact pressure of 30-40 PSI is adequate to secure the thermal management device and to achieve the lowest thermal contact resistance with a temperature drop across the thermal interface material of no more than 3°C. Also, the surface flatness of the metal spreader should be 0.001 inch/1 inch.
- Pre-test the assembly fixture with a strain gauge to ensure that the flexing of the final assembled board and the pressure applying around the GPU package will not exceed 600-micron strain under any circumstance. For strain gauge setup and test methodology, refer to industrial standards (IPC/JEDEC-9704 - Printed Wiring Board Strain Gauge Test Guideline).
- Ensure that any distortion (bow or twist) of the board after SMT and cooling device assembly is within industry guidelines (IPC/EIA J-STD-001). For the measurement method, refer to the industry approved technique described in the manual, *IPC-TM-650*, section 2.4.22.

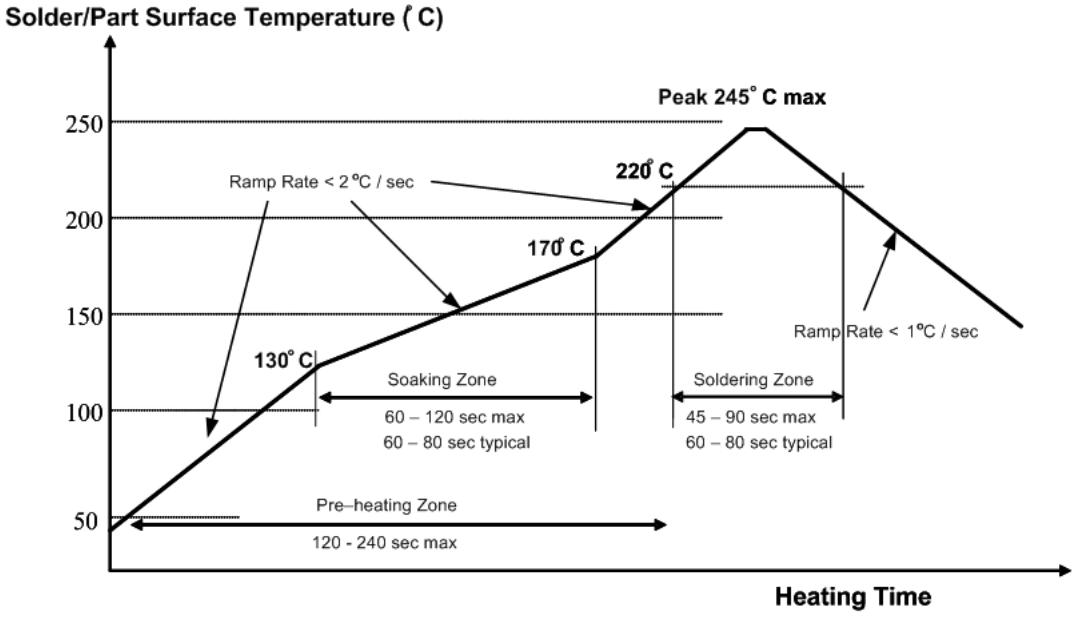
7.3 Board Solder Reflow Process Recommendations

7.3.1 Stencil Opening Size for Solderball Pads on PCB

Warpage of the PCB and the BGA package may cause solder-joint quality issues at the surface mount. Therefore, it is recommended that the stencil opening sizes be adjusted to compensate for the warpage. The recommendation is for the stencil aperture of BGA balls to be kept as the same size as the PWB BGA pad design.

7.3.2 FCBGA Reference Reflow Profile for RoHS/Lead-free Solder

Figure 7–4 FCBGA Reference Reflow Profile for RoHS/Lead-Free SMT



Notes when using RoHS/lead-free solder (SAC305 Tin-Silver-Cu):

- The final reflow temperature profile will depend on the type of solder paste and chemistry of flux used in the SMT process or BGA rework process. Modifications to this reference reflow profile may also be required in order to accommodate to other critical components.
- The use of a reflow oven with 10 heating zones or above is highly recommended.
- To ensure that the reflow profile meets the target specification on both sides of SMT components, a different reflow profile for the first and second reflow may be required.
- A mechanical stiffening carrier boat can be used to minimize PWB warpage during the reflow process.
- It is suggested to decrease the temperature cooling rate to minimize BGA component and PWB warpage.
- This recommended reflow profile applies only to the RoHS/lead-free (high temperature) soldering process, and it should not be applied to Eutectic solder packages without any reliability validation.
- Maximum three reflows are allowed on the same part.

Table 7–1 Recommended Profiling — RoHS/Lead-Free Solder

Profiling Stage	Temperature	Process Range
Overall Preheat	Room temperature to 220℃	Two to four minutes
Soaking Time	130℃ to 170℃	Typically 60 to 80 seconds
Liquidus	220℃	Typically 60 to 80 seconds
Ramp Rate	Ramp up	< 2℃ / second
	Ramp down	< 1℃ / second
Peak	Maximum 245℃	235℃ ± 5℃
Temperature at Peak Within 5℃	240℃ to 245℃	10 to 30 seconds

8

Boundary Scan Specification

This chapter contains information on boundary scan specifications as they apply to "Vega 10". To go to a topic of interest, use the following list of linked cross-references:

8.1 Introduction

"Vega 10" has a JTAG 1149.1 compliant TAP controller. The boundary scan implementation is IEEE compliant. The implementation supports BYPASS, EXTEST, and PRELOAD instructions. A BSDL file for each of the modes can be obtained from the AMD OEM Resource Center.

8.2 Boundary Scan

The "Vega 10" boundary scan can perform board-level capture and drive out on all pins mentioned in the BSDL file.

8.3 JTAG Interface Signals

Table 8–1 JTAG Interface

Pin-name	I/O	Description
JTAG_TCK	I	TCK: Test clock.
JTAG_TMS	I	TMS: Test mode select.
JTAG_TDI	I	TDI: Test data in.
JTAG_TDO	O	TDO: Test data out.
JTAG_TRSTB	I	TRST#: Test asynchronous reset.
TESTEN	I	Compliance pin: Pull up to 3.3 V to enable JTAG access.

8.4 JTAG Timing Characteristics

Table 8–2 JTAG Timing Characteristics

Symbol	Description	Min	Max
$\mathbf{f_{cyc}}$	Frequency of operation.	0.001 MHz	10 MHz
$\mathbf{t_{cyc}}$	TCK cycle period.	0.10 µs	1000 µs
$\mathbf{t_{bsst}}$	Input data setup time to TCK rise.	15 ns	
$\mathbf{t_{bsht}}$	Input data hold time to TCK rise.	20 ns	
$\mathbf{t_{bsdv}}$	TCK low to output data valid.	0.00 µs	0.05 µs
$\mathbf{t_{tcst}}$	TDI, TMS setup time to TCK rise.	2.5 ns	
$\mathbf{t_{tcht}}$	TDI, TMS hold time to TCK rise.	3.0 ns	
$\mathbf{t_{tcdv}}$	TCK low to TDO data valid.	0.0 µs	0.05 µs

Figure 8–1 Timing of the Boundary Scan Signals with Respect to TCK

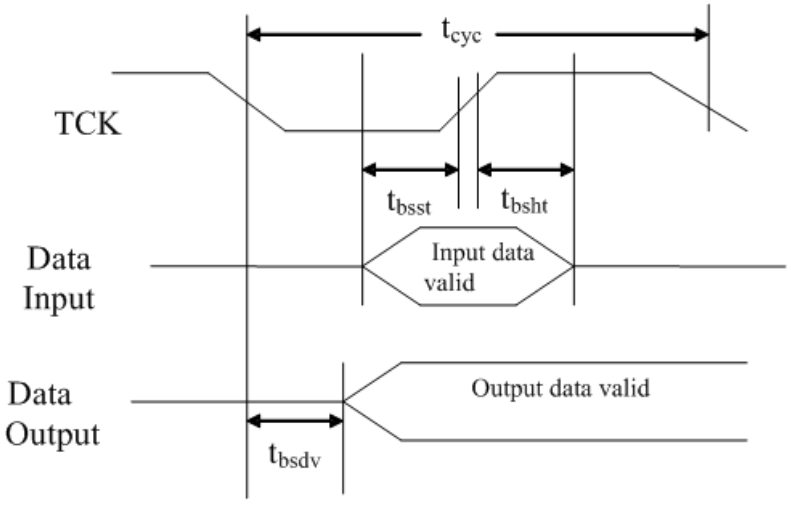
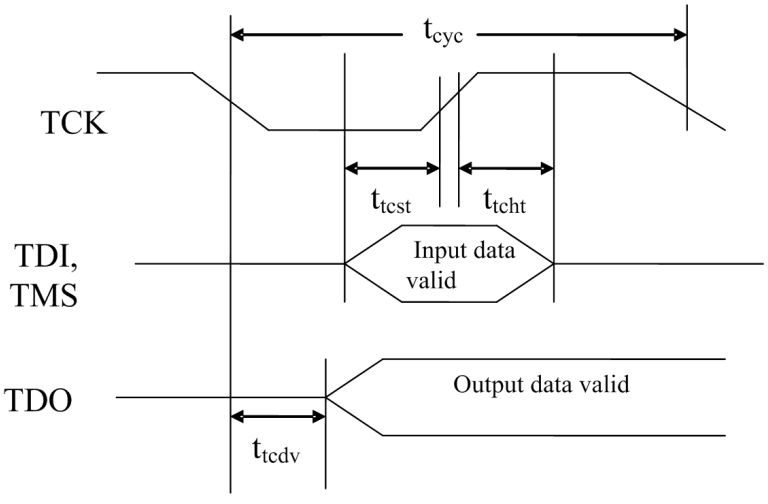


Figure 8–2 Timing of the TAP Ports (TDI, TMS, and TDO) with Respect to TCK



Appendix A

Pin Listings

This appendix contains pin listings for "Vega 10" sorted in two ways. To go to the listing of interest, use the following list of linked cross-references:

- Pins Sorted by Ball Reference (p. 79)
- Pins Sorted by Signal Name (p. 127)

A.1 Pins Sorted by Ball Reference

Table A–1 Pins Sorted by Ball Reference

Ball Reference	Signal Name
A2	VDDCR_SOC
A3	VDDCR_SOC
A4	VDDCR_SOC
A6	VDDCR_SOC
A7	VDDCR_SOC
A8	VDDCR_SOC
A9	VDDCR_SOC
A10	VDDCR_SOC
A11	VDDCR_SOC
A12	VDDCR_SOC
A13	VDDCR_SOC
A14	VDDCR_SOC
A15	VDDCR_SOC
A16	VDDCR_SOC
A17	VDDCR_SOC
A18	VDDCR_SOC
A19	VDDCR_SOC
A20	VDDCR_SOC
A21	VDDCR_SOC
A22	VDDCR_SOC
A23	VDDCR_SOC
A24	VDDCR_SOC
A25	VDDCR_SOC
A26	VDDCR_SOC
A27	VDDCR_SOC
A28	VDDCR_SOC

Ball Reference	Signal Name
A29	VDDCR_SOC
A30	VDDCR_SOC
A31	VDDCR_SOC
A32	VDDCR_SOC
A33	VDDCR_SOC
A34	VDDCR_SOC
A35	VDDCR_SOC
A36	VDDCR_SOC
A37	VDDCR_SOC
A38	VDDCR_SOC
A39	VDDCR_SOC
A40	VDDCR_SOC
A42	VDDCR_SOC
A43	VDDCR_SOC
A44	VDDCR_SOC
B1	RSVD
B2	DFTIO_29
B3	VSS
B4	DFTIO_44
B5	DFTIO_31
B6	DFTIO_48
B7	VSS
B8	DFTIO_58
B9	DFTIO_68
B10	VDDCR_SOC
B11	VSS
B12	RSVD
B13	DFTIO_86
B14	DFTIO_91
B15	VDDCR_SOC
B16	DFTIO_97
B17	DFTIO_107
B18	DFTIO_109
B19	VDDCR_SOC
B20	DFTIO_112
B21	DFTIO_120
B22	DFTIO_121
B23	VDDCR_SOC
B24	DFTIO_135
B25	DFTIO_136
B26	DFTIO_143
B27	VDDCR_SOC

Ball Reference	Signal Name
B28	DFTIO_152
B29	DFTIO_158
B30	DFTIO_161
B31	VDDCR_SOC
B32	DFTIO_165
B33	DFTIO_166
B34	DFTIO_174
B35	VDDCR_SOC
B36	DFTIO_210
B37	DFTIO_211
B38	DFTIO_203
B39	VSS
B40	DFTIO_201
B41	DFTIO_202
B42	DFTIO_209
B43	VSS
B44	DFTIO_187
B45	VDDCR_SOC
C1	DFTIO_17
C2	DFTIO_9
C3	DFTIO_21
C4	DFTIO_22
C5	VSS
C6	DFTIO_32
C7	DFTIO_49
C8	DFTIO_52
C9	VSS
C10	DFTIO_75
C11	DFTIO_87
C12	RSVD
C13	VSS
C14	DFTIO_74
C15	DFTIO_82
C16	DFTIO_85
C17	VSS
C18	DFTIO_96
C19	DFTIO_102
C20	DFTIO_104
C21	VSS
C22	DFTIO_115
C23	DFTIO_119
C24	DFTIO_129

Ball Reference	Signal Name
C25	VSS
C26	DFTIO_118
C27	DFTIO_131
C28	DFTIO_139
C29	VSS
C30	DFTIO_153
C31	DFTIO_133
C32	DFTIO_147
C33	VSS
C34	DFTIO_151
C35	DFTIO_167
C36	DFTIO_175
C37	VSS
C38	DFTIO_169
C39	DFTIO_222
C40	DFTIO_217
C41	VSS
C42	DFTIO_204
C43	DFTIO_182
C44	DFTIO_189
C45	VDDCR_SOC
D1	VSS
D2	DFTIO_18
D3	DFTIO_27
D4	DFTIO_13
D5	DFTIO_33
D6	DFTIO_39
D7	VSS
D8	DFTIO_36
D9	DFTIO_47
D10	DFTIO_70
D11	VSS
D12	RSVD
D13	DFTIO_65
D14	DFTIO_77
D15	VDDCR_SOC
D16	DFTIO_92
D17	DFTIO_101
D18	DFTIO_105
D19	VDDCR_SOC
D20	DFTIO_108
D21	DFTIO_110

Ball Reference	Signal Name
D22	DFTIO_116
D23	VDDCR_SOC
D24	DFTIO_128
D25	DFTIO_132
D26	DFTIO_146
D27	VDDCR_SOC
D28	DFTIO_137
D29	DFTIO_142
D30	DFTIO_154
D31	VDDCR_SOC
D32	DFTIO_162
D33	DFTIO_179
D34	DFTIO_190
D35	VDDCR_SOC
D36	DFTIO_149
D37	DFTIO_181
D38	DFTIO_164
D39	VSS
D40	DFTIO_172
D41	DFTIO_192
D42	DFTIO_180
D43	VSS
D44	DFTIO_186
D45	VDDCR_SOC
E2	VSS
E3	DFTIO_5
E4	DFTIO_2
E5	VSS
E6	DFTIO_12
E7	DFTIO_16
E8	DFTIO_34
E9	VSS
E10	DFTIO_64
E11	DFTIO_56
E12	DFTIO_55
E13	VSS
E14	DFTIO_62
E15	DFTIO_79
E16	DFTIO_84
E17	VSS
E18	DFTIO_94
E19	DFTIO_111

Ball Reference	Signal Name
E20	DFTIO_117
E21	VSS
E22	DFTIO_106
E23	DFTIO_126
E24	DFTIO_141
E25	VSS
E26	DFTIO_176
E27	DFTIO_177
E28	DFTIO_157
E29	VSS
E30	DFTIO_148
E31	DFTIO_163
E32	DFTIO_173
E33	VSS
E34	DFTIO_208
E35	DFTIO_214
E36	DFTIO_221
E37	VSS
E38	DFTIO_219
E39	DFTIO_216
E40	DFTIO_228
E41	VSS
E42	DFTIO_194
E43	DFTIO_199
E44	DFTIO_188
F1	VSS
F2	TXCFP_DPF3P
F3	TXCFM_DPF3N
F4	VSS
F5	DDC1DATA
F6	DDC1CLK
F7	VSS
F8	DFTIO_25
F9	DFTIO_53
F10	DFTIO_38
F11	VSS
F12	DFTIO_46
F13	DFTIO_50
F14	DFTIO_61
F15	VDDCR_SOC
F16	DFTIO_89
F17	DFTIO_95

Ball Reference	Signal Name
F18	DFTIO_103
F19	VDDCR_SOC
F20	DFTIO_127
F21	DFTIO_138
F22	DFTIO_122
F23	VDDCR_SOC
F24	DFTIO_145
F25	DFTIO_134
F26	DFTIO_159
F27	VDDCR_SOC
F28	DFTIO_168
F29	DFTIO_183
F30	DFTIO_196
F31	VDDCR_SOC
F32	DFTIO_185
F33	DFTIO_220
F34	DFTIO_206
F35	VDDCR_SOC
F36	DFTIO_254
F37	DFTIO_243
F38	DFTIO_235
F39	VSS
F40	DFTIO_200
F41	DFTIO_229
F42	DFTIO_195
F43	VSS
F44	DFTIO_215
F45	VDDCR_SOC
G1	TX0P_DPF2P
G2	TX0M_DPF2N
G3	VSS
G4	AUX1P
G5	AUX1N
G6	VSS
G7	HPD1
G8	DFTIO_28
G9	VSS
G10	DFTIO_42
G11	DFTIO_57
G12	DFTIO_45
G13	VSS
G14	DFTIO_63

Ball Reference	Signal Name
G15	DFTIO_83
G16	DFTIO_80
G17	VSS
G18	DFTIO_76
G19	DFTIO_88
G20	DFTIO_98
G21	VSS
G22	DFTIO_81
G23	DFTIO_114
G24	DFTIO_93
G25	VSS
G26	DFTIO_123
G27	DFTIO_144
G28	DFTIO_130
G29	VSS
G30	DFTIO_171
G31	DFTIO_156
G32	DFTIO_212
G33	VSS
G34	DFTIO_252
G35	DFTIO_234
G36	DFTIO_227
G37	VSS
G38	DFTIO_257
G39	DFTIO_245
G40	DFTIO_244
G41	VSS
G42	DFTIO_223
G43	DFTIO_224
G44	DFTIO_205
G45	VDDCR_SOC
H1	VSS
H2	TX1P_DPF1P
H3	TX1M_DPF1N
H4	VSS
H5	VDDAN_33
H6	VDDAN_33
H7	VSS
H8	DFTIO_20
H9	DFTIO_43
H10	DFTIO_30
H11	VSS

Ball Reference	Signal Name
H12	DFTIO_59
H13	DFTIO_69
H14	DFTIO_73
H15	VDDCR_SOC
H16	DFTIO_60
H17	DFTIO_71
H18	DFTIO_67
H19	VDDCR_SOC
H20	DFTIO_66
H21	DFTIO_72
H22	DFTIO_78
H23	VDDCR_SOC
H24	DFTIO_155
H25	DFTIO_170
H26	DFTIO_113
H27	VDDCR_SOC
H28	DFTIO_178
H29	DFTIO_191
H30	DFTIO_198
H31	VDDCR_SOC
H32	DFTIO_290
H33	DFTIO_281
H34	DFTIO_238
H35	VDDCR_SOC
H36	DFTIO_218
H37	DFTIO_207
H38	DFTIO_269
H39	VDDCR_SOC
H40	DFTIO_272
H41	DFTIO_249
H42	DFTIO_226
H43	VDDCR_SOC
H44	DFTIO_225
H45	VDDCR_SOC
J1	TX2P_DPF0P
J2	TX2M_DPF0N
J3	VSS
J4	DDC2DATA
J5	DDC2CLK
J6	VSS
J7	DFTIO_0
J8	DFTIO_26

Ball Reference	Signal Name
J9	VSS
J10	DFTIO_35
J11	DFTIO_37
J12	DFTIO_41
J13	VDDCR_SOC
J14	DFTIO_40
J15	DFTIO_54
J16	DFTIO_51
J17	VDDCR_SOC
J18	DFTIO_90
J19	DFTIO_100
J20	DFTIO_99
J21	VDDCR_SOC
J22	DFTIO_125
J23	DFTIO_150
J24	DFTIO_160
J25	VDDCR_SOC
J26	DFTIO_124
J27	DFTIO_140
J28	DFTIO_184
J29	VDDCR_SOC
J30	DFTIO_197
J31	DFTIO_213
J32	DFTIO_232
J33	VDDCR_SOC
J34	DFTIO_247
J35	DFTIO_193
J36	DFTIO_255
J37	VSS
J38	DFTIO_264
J39	DFTIO_256
J40	DFTIO_259
J41	VSS
J42	DFTIO_242
J43	DFTIO_230
J44	DFTIO_231
J45	VDDCR_SOC
K1	VSS
K2	AUX2P
K3	AUX2N
K4	VSS
K5	GENERICC_HPD2

Ball Reference	Signal Name
K6	VDDAN_33
K7	VSS
K8	DFTIO_23
K9	DFTIO_14
K10	DFTIO_19
K11	VSS
K12	VSS
K13	VDDCR_SOC
K14	VDDCR_SOC
K15	VSS
K16	VSS
K17	VDDCR_SOC
K18	VDDCR_SOC
K19	VSS
K20	VSS
K21	VDDCR_SOC
K22	VDDCR_SOC
K23	VSS
K24	VSS
K25	VDDCR_SOC
K26	VDDCR_SOC
K27	VSS
K28	VSS
K29	VDDCR_SOC
K30	VDDCR_SOC
K31	VSS
K32	VSS
K33	VDDCR_SOC
K34	VDDCR_SOC
K35	VSS
K36	VSS
K37	DFTIO_265
K38	DFTIO_286
K39	VDDCR_SOC
K40	DFTIO_246
K41	DFTIO_239
K42	DFTIO_241
K43	VDDCR_SOC
K44	DFTIO_233
K45	VDDCR_SOC
L1	TXCEP_DPE3P
L2	TXCEM_DPE3N

Ball Reference	Signal Name
L3	VSS
L4	RSVD
L5	VSS
L6	VDDAN_33
L7	DFTIO_7
L8	DFTIO_3
L9	VSS
L10	DFTIO_24
L11	DFTIO_1
L12	VSS
L13	VDDCR_SOC
L14	VDDCR_SOC
L15	VSS
L16	VSS
L17	VDDCR_SOC
L18	VDDCR_SOC
L19	VSS
L20	VSS
L21	VDDCR_SOC
L22	VDDCR_SOC
L23	VSS
L24	VSS
L25	VDDCR_SOC
L26	VDDCR_SOC
L27	VSS
L28	VSS
L29	VDDCR_SOC
L30	VDDCR_SOC
L31	VSS
L32	VSS
L33	VDDCR_SOC
L34	VDDCR_SOC
L35	VDDCR_SOC
L36	VDDCR_SOC
L37	VDDCR_SOC
L38	DFTIO_280
L39	DFTIO_289
L40	DFTIO_276
L41	VDDCR_SOC
L42	DFTIO_248
L43	DFTIO_240
L44	DFTIO_237

Ball Reference	Signal Name
L45	VDDCR_SOC
M1	VSS
M2	TX3P_DPE2P
M3	TX3M_DPE2N
M4	VSS
M5	VDDAN_18
M6	VDDAN_18
M7	VSS
M8	DFTIO_11
M9	DFTIO_6
M10	DFTIO_4
M11	VSS
M12	VSS
M13	VDDCR_SOC
M14	VDDCR_SOC
M15	VSS
M16	VSS
M17	VDDCR_SOC
M18	VDDCR_SOC
M19	VSS
M20	VSS
M21	VDDCR_SOC
M22	VDDCR_SOC
M23	VSS
M24	VSS
M25	VDDCR_SOC
M26	VDDCR_SOC
M27	VSS
M28	VSS
M29	VDDCR_SOC
M30	VDDCR_SOC
M31	VSS
M32	VSS
M33	VDDCR_SOC
M34	VDDCR_SOC
M35	VDDCR_SOC
M36	VDDCR_SOC
M37	DFTIO_275
M38	DFTIO_310
M39	VDDCR_SOC
M40	DFTIO_282
M41	DFTIO_261

Ball Reference	Signal Name
M42	DFTIO_253
M43	VDDCR_SOC
M44	DFTIO_236
M45	VDDCR_SOC
N1	TX4P_DPE1P
N2	TX4M_DPE1N
N3	VSS
N4	VDDAN_18
N5	VSS
N6	VDDAN_18
N7	RSVD
N8	DFTIO_8
N9	VSS
N10	DFTIO_10
N11	RSVD
N12	VSS
N13	VDDCR_SOC
N14	VDDCR_SOC
N15	VSS
N16	VSS
N17	VDDCR_SOC
N18	VDDCR_SOC
N19	VSS
N20	VSS
N21	VDDCR_SOC
N22	VDDCR_SOC
N23	VSS
N24	VSS
N25	VDDCR_SOC
N26	VDDCR_SOC
N27	VSS
N28	VSS
N29	VDDCR_SOC
N30	VDDCR_SOC
N31	VSS
N32	VSS
N33	VSS
N34	VSS
N35	VSS
N36	VSS
N37	VSS
N38	DFTIO_320

Ball Reference	Signal Name
N39	DFTIO_300
N40	DFTIO_287
N41	VSS
N42	DFTIO_260
N43	DFTIO_250
N44	DFTIO_251
N45	VDDCR_SOC
P1	VSS
P2	TX5P_DPE0P
P3	TX5M_DPE0N
P4	VSS
P5	AUX_ZVSS
P6	GENERICD_HPD3
P7	VSS
P8	RSVD
P9	DFTIO_15
P10	RSVD
P11	VSS
P12	VSS
P13	VDDCR_SOC
P14	VDDCR_SOC
P15	VSS
P16	VSS
P17	VDDCR_SOC
P18	VDDCR_SOC
P19	VSS
P20	VSS
P21	VDDCR_SOC
P22	VDDCR_SOC
P23	VSS
P24	VSS
P25	VDDCR_SOC
P26	VDDCR_SOC
P27	VSS
P28	VSS
P29	VDDCR_SOC
P30	VDDCR_SOC
P31	VSS
P32	VSS
P33	VSS
P34	VSS
P35	VSS

Ball Reference	Signal Name
P36	VSS
P37	DFTIO_295
P38	DFTIO_324
P39	VSS
P40	DFTIO_301
P41	DFTIO_288
P42	DFTIO_267
P43	VSS
P44	DFTIO_258
P45	VDDCR_SOC
R1	TXCDP_DPD3P
R2	TXCDM_DPD3N
R3	VSS
R4	DDCAUX3P
R5	DDCAUX3N
R6	VSS
R7	GENLK_CLK
R8	GENLK_VSYNC
R9	VSS
R10	RSVD
R11	RSVD
R12	VSS
R13	VDDCR_SOC
R14	VDDCR_SOC
R15	VSS
R16	VSS
R17	VDDCR_SOC
R18	VDDCR_SOC
R19	VSS
R20	VSS
R21	VDDCR_SOC
R22	VDDCR_SOC
R23	VSS
R24	VSS
R25	VDDCR_SOC
R26	VDDCR_SOC
R27	VSS
R28	VSS
R29	VDDCR_SOC
R30	VDDCR_SOC
R31	VDDCR_SOC
R32	VDDCR_SOC

Ball Reference	Signal Name
R33	VDDCR_SOC
R34	VDDCR_SOC
R35	VDDCR_SOC
R36	VDDCR_SOC
R37	VDDCR_SOC
R38	DFTIO_315
R39	DFTIO_270
R40	DFTIO_309
R41	VDDCR_SOC
R42	DFTIO_284
R43	DFTIO_262
R44	DFTIO_263
R45	VDDCR_SOC
T1	VSS
T2	TX0P_DPD2P
T3	TX0M_DPD2N
T4	VSS
T5	SWAPLOCKA
T6	SWAPLOCKB
T7	VSS
T8	GPIO_0
T9	GPIO_SVD0
T10	RSVD
T11	VSS
T12	VSS
T13	VDDCR_SOC
T14	VDDCR_SOC
T15	VSS
T16	VSS
T17	VDDCR_SOC
T18	VDDCR_SOC
T19	VSS
T20	VSS
T21	VDDCR_SOC
T22	VDDCR_SOC
T23	VSS
T24	VSS
T25	VDDCR_SOC
T26	VDDCR_SOC
T27	VSS
T28	VSS
T29	VDDCR_SOC

Ball Reference	Signal Name
T30	VDDCR_SOC
T31	VDDCR_SOC
T32	VDDCR_SOC
T33	VDDCR_SOC
T34	VDDCR_SOC
T35	VDDCR_SOC
T36	VDDCR_SOC
T37	TEST6
T38	DFTIO_322
T39	VDDCR_SOC
T40	DFTIO_303
T41	DFTIO_277
T42	DFTIO_268
T43	VDDCR_SOC
T44	DFTIO_285
T45	VDDCR_SOC
U1	TX1P_DPD1P
U2	TX1M_DPD1N
U3	VSS
U4	RSVD
U5	RSVD
U6	VSS
U7	GPIO_1
U8	GPIO_SVT0
U9	VSS
U10	RSVD
U11	RSVD
U12	VSS
U13	VDDCR_SOC
U14	VDDCR_SOC
U15	VSS
U16	VSS
U17	VDDCR_SOC
U18	VDDCR_SOC
U19	VSS
U20	VSS
U21	VDDCR_SOC
U22	VDDCR_SOC
U23	VSS
U24	VSS
U25	VDDCR_SOC
U26	VDDCR_SOC

Ball Reference	Signal Name
U27	VSS
U28	VSS
U29	VSS
U30	VSS
U31	VSS
U32	VSS
U33	VSS
U34	VSS
U35	VSS
U36	VSS
U37	VSS
U38	DFTIO_278
U39	DFTIO_279
U40	DFTIO_308
U41	VSS
U42	DFTIO_271
U43	DFTIO_298
U44	DFTIO_296
U45	VDDCR_SOC
V1	VSS
V2	TX2P_DPD0P
V3	TX2M_DPD0N
V4	VSS
V5	GENERICE_HPD4
V6	GPIO_9_ROMSO
V7	GPIO_2
V8	VSS
V9	GPIO_SVC0
V10	INTCRACKMONGLL
V11	VSS
V12	VSS
V13	VDDCR_SOC
V14	VDDCR_SOC
V15	VSS
V16	VSS
V17	VDDCR_SOC
V18	VDDCR_SOC
V19	VSS
V20	VSS
V21	VDDCR_SOC
V22	VDDCR_SOC
V23	VSS

Ball Reference	Signal Name
V24	VSS
V25	VDDCR_SOC
V26	VDDCR_SOC
V27	VSS
V28	VSS
V29	VSS
V30	VSS
V31	VSS
V32	VSS
V33	VSS
V34	VSS
V35	VSS
V36	VSS
V37	INTCRACKMONGUL
V38	DFTIO_283
V39	VSS
V40	DFTIO_299
V41	DFTIO_273
V42	DFTIO_274
V43	VSS
V44	DFTIO_266
V45	VDDCR_SOC
W1	TXCCP_DPC3P
W2	TXCCM_DPC3N
W3	VSS
W4	DDCAUX4P
W5	DDCAUX4N
W6	VSS
W7	GPIO_7_ROMSCK
W8	GPIO_8_ROMSI
W9	VSS
W10	RSVD
W11	RSVD
W12	VSS
W13	VDDCR_SOC
W14	VDDCR_SOC
W15	VSS
W16	VSS
W17	VDDCR_SOC
W18	VDDCR_SOC
W19	VSS
W20	VSS

Ball Reference	Signal Name
W21	VDDCR_SOC
W22	VDDCR_SOC
W23	VSS
W24	VSS
W25	VDDCR_SOC
W26	VDDCR_SOC
W27	VDDCR_SOC
W28	VDDCR_SOC
W29	VDDCR_SOC
W30	VDDCR_SOC
W31	VDDCR_SOC
W32	VDDCR_SOC
W33	VDDCR_SOC
W34	VDDCR_SOC
W35	VDDCR_SOC
W36	VDDCR_SOC
W37	VDDCR_SOC
W38	DFTIO_291
W39	DFTIO_292
W40	DFTIO_293
W41	VDDCR_SOC
W42	DFTIO_304
W43	DFTIO_306
W44	DFTIO_297
W45	VDDCR_SOC
Y1	VSS
Y2	TX3P_DPC2P
Y3	TX3M_DPC2N
Y4	VSS
Y5	VDD_18
Y6	VDD_18
Y7	GPIO_10_ROMCSB
Y8	VSS
Y9	RSVD
Y10	INTCRACKMONGLR
Y11	VSS
Y12	VSS
Y13	VDDCR_SOC
Y14	VDDCR_SOC
Y15	VSS
Y16	VSS
Y17	VDDCR_SOC

Ball Reference	Signal Name
Y18	VDDCR_SOC
Y19	VSS
Y20	VSS
Y21	VDDCR_SOC
Y22	VDDCR_SOC
Y23	VSS
Y24	VSS
Y25	VDDCR_SOC
Y26	VDDCR_SOC
Y27	VDDCR_SOC
Y28	VDDCR_SOC
Y29	VDDCR_SOC
Y30	VDDCR_SOC
Y31	VDDCR_SOC
Y32	VDDCR_SOC
Y33	VDDCR_SOC
Y34	VDDCR_SOC
Y35	VDDCR_SOC
Y36	VDDCR_SOC
Y37	INTCRACKMONGUR
Y38	DFTIO_294
Y39	VDDCR_SOC
Y40	DFTIO_316
Y41	DFTIO_323
Y42	DFTIO_305
Y43	VDDCR_SOC
Y44	DFTIO_302
Y45	VDDCR_SOC
AA1	TX4P_DPC1P
AA2	TX4M_DPC1N
AA3	VSS
AA4	RSVD
AA5	VDD_18
AA6	VSS
AA7	RSVD
AA8	TRST_L
AA9	VSS
AA10	RSVD
AA11	RSVD
AA12	VSS
AA13	VDDCR_SOC
AA14	VDDCR_SOC

Ball Reference	Signal Name
AA15	VSS
AA16	VSS
AA17	VDDCR_SOC
AA18	VDDCR_SOC
AA19	VSS
AA20	VSS
AA21	VDDCR_SOC
AA22	VDDCR_SOC
AA23	VSS
AA24	VSS
AA25	VSS
AA26	VSS
AA27	VSS
AA28	VSS
AA29	VSS
AA30	VSS
AA31	VSS
AA32	VSS
AA33	VSS
AA34	VSS
AA35	VSS
AA36	VSS
AA37	VSS
AA38	DFTIO_329
AA39	DFTIO_318
AA40	DFTIO_321
AA41	VSS
AA42	DFTIO_312
AA43	DFTIO_313
AA44	DFTIO_307
AA45	VDDCR_SOC
AB1	VSS
AB2	TX5P_DPC0P
AB3	TX5M_DPC0N
AB4	VSS
AB5	VDD_18
AB6	VDD_18
AB7	VSS
AB8	TDO
AB9	TDI
AB10	RSVD
AB11	VSS

Ball Reference	Signal Name
AB12	VSS
AB13	VDDCR_SOC
AB14	VDDCR_SOC
AB15	VSS
AB16	VSS
AB17	VDDCR_SOC
AB18	VDDCR_SOC
AB19	VSS
AB20	VSS
AB21	VDDCR_SOC
AB22	VDDCR_SOC
AB23	VSS
AB24	VSS
AB25	VSS
AB26	VSS
AB27	VSS
AB28	VSS
AB29	VSS
AB30	VSS
AB31	VSS
AB32	VSS
AB33	VSS
AB34	VSS
AB35	VSS
AB36	VSS
AB37	DFTIO_332
AB38	DFTIO_335
AB39	VSS
AB40	DFTIO_317
AB41	DFTIO_314
AB42	DFTIO_325
AB43	VSS
AB44	DFTIO_311
AB45	VDDCR_SOC
AC1	TXCBP_DPB3P
AC2	TXCBM_DPB3N
AC3	VSS
AC4	GENERICF_HPD5
AC5	VSS
AC6	VDD_18
AC7	TMS
AC8	TCK

Ball Reference	Signal Name
AC9	VSS
AC10	RSVD
AC11	RSVD
AC12	VSS
AC13	VDDCR_SOC
AC14	VDDCR_SOC
AC15	VSS
AC16	VSS
AC17	VDDCR_SOC
AC18	VDDCR_SOC
AC19	VSS
AC20	VSS
AC21	VDDCR_SOC
AC22	VDDCR_SOC
AC23	VDDCR_SOC
AC24	VDDCR_SOC
AC25	VDDCR_SOC
AC26	VDDCR_SOC
AC27	VDDCR_SOC
AC28	VDDCR_SOC
AC29	VDDCR_SOC
AC30	VDDCR_SOC
AC31	VDDCR_SOC
AC32	VDDCR_SOC
AC33	VDDCR_SOC
AC34	VDDCR_SOC
AC35	VDDCR_SOC
AC36	VDDCR_SOC
AC37	VDDCR_SOC
AC38	DFTIO_334
AC39	DFTIO_326
AC40	DFTIO_319
AC41	VDDCR_SOC
AC42	DFTIO_333
AC43	DFTIO_330
AC44	DFTIO_328
AC45	VDDCR_SOC
AD1	VSS
AD2	TX0P_DPB2P
AD3	TX0M_DPB2N
AD4	VSS
AD5	DDCAUX5P

Ball Reference	Signal Name
AD6	DDCAUX5N
AD7	VSS
AD8	TESTEN
AD9	XTRIG6
AD10	RSVD
AD11	VSS
AD12	VSS
AD13	VDDCR_SOC
AD14	VDDCR_SOC
AD15	VSS
AD16	VSS
AD17	VDDCR_SOC
AD18	VDDCR_SOC
AD19	VSS
AD20	VSS
AD21	VDDCR_SOC
AD22	VDDCR_SOC
AD23	VDDCR_SOC
AD24	VDDCR_SOC
AD25	VDDCR_SOC
AD26	VDDCR_SOC
AD27	VDDCR_SOC
AD28	VDDCR_SOC
AD29	VDDCR_SOC
AD30	VDDCR_SOC
AD31	VDDCR_SOC
AD32	VDDCR_SOC
AD33	VDDCR_SOC
AD34	VDDCR_SOC
AD35	VDDCR_SOC
AD36	VDDCR_SOC
AD37	RSVD
AD38	RSVD
AD39	VDDCR_SOC
AD40	RSVD
AD41	DFTIO_327
AD42	DFTIO_331
AD43	VDDCR_SOC
AD44	RSVD
AD45	VDDCR_SOC
AE1	TX1P_DPB1P
AE2	TX1M_DPB1N

Ball Reference	Signal Name
AE3	VSS
AE4	GENERICG_HPD6
AE5	VSS
AE6	VDD_18
AE7	GPIO_5
AE8	GPIO_6
AE9	VSS
AE10	INTCRACKMONDA
AE11	RSVD
AE12	VSS
AE13	VDDCR_SOC
AE14	VDDCR_SOC
AE15	VSS
AE16	VSS
AE17	VDDCR_SOC
AE18	VDDCR_SOC
AE19	VSS
AE20	VSS
AE21	VSS
AE22	VSS
AE23	VSS
AE24	VSS
AE25	VSS
AE26	VSS
AE27	VSS
AE28	VSS
AE29	VSS
AE30	VSS
AE31	VSS
AE32	VSS
AE33	VSS
AE34	VSS
AE35	VSS
AE36	VSS
AE37	VSS
AE38	RSVD
AE39	RSVD
AE40	RSVD
AE41	VSS
AE42	RSVD
AE43	RSVD
AE44	RSVD

Ball Reference	Signal Name
AE45	VDDCR_SOC
AF1	VSS
AF2	TX2P_DPB0P
AF3	TX2M_DPB0N
AF4	VSS
AF5	DDCAUX6P
AF6	DDCAUX6N
AF7	VSS
AF8	VDDAN_Q_EFUSE
AF9	VDDAN_Q_EFUSE
AF10	RSVD
AF11	VSS
AF12	VSS
AF13	VSS
AF14	VSS
AF15	VSS
AF16	VSS
AF17	VDDCR_SOC
AF18	VDDCR_SOC
AF19	VSS
AF20	VSS
AF21	VSS
AF22	VSS
AF23	VSS
AF24	VSS
AF25	VSS
AF26	VSS
AF27	VSS
AF28	VSS
AF29	VSS
AF30	VSS
AF31	VSS
AF32	VSS
AF33	VSS
AF34	VSS
AF35	VSS
AF36	VSS
AF37	RSVD
AF38	RSVD
AF39	VSS
AF40	RSVD
AF41	RSVD

Ball Reference	Signal Name
AF42	RSVD
AF43	VSS
AF44	RSVD
AF45	VDDCR_SOC
AG1	TXCAP_DPA3P
AG2	TXCAM_DPA3N
AG3	VSS
AG4	VDD_18
AG5	VDD_18
AG6	DP_ZVSS
AG7	GPIO_4
AG8	GPIO_3
AG9	XTRIG7
AG10	VDDCR_BACO
AG11	VDDCR_BACO
AG12	VSS
AG13	VSS
AG14	VSS
AG15	VSS
AG16	VSS
AG17	VDDCR_SOC
AG18	VDDCR_SOC
AG19	VDDCR_SOC
AG20	VDDCR_SOC
AG21	VDDCR_SOC
AG22	VDDCR_SOC
AG23	VDDCR_SOC
AG24	VDDCR_SOC
AG25	VDDCR_SOC
AG26	VDDCR_SOC
AG27	VDDCR_SOC
AG28	VDDCR_SOC
AG29	VDDCR_SOC
AG30	VDDCR_SOC
AG31	VDDCR_SOC
AG32	VDDCR_SOC
AG33	VDDCR_SOC
AG34	VDDCR_SOC
AG35	VDDCR_SOC
AG36	VDDCR_SOC
AG37	VDDCR_SOC
AG38	RSVD

Ball Reference	Signal Name
AG39	RSVD
AG40	RSVD
AG41	VDDCR_SOC
AG42	RSVD
AG43	RSVD
AG44	RSVD
AG45	VDDCR_SOC
AH1	VSS
AH2	TX3P_DPA2P
AH3	TX3M_DPA2N
AH4	VSS
AH5	VDD_18
AH6	DP_ZVDD_08
AH7	VSS
AH8	VSS
AH9	VDDCR_BACO
AH10	VDDCR_BACO
AH11	VSS
AH12	VSS
AH13	VSS
AH14	VSS
AH15	VSS
AH16	VSS
AH17	FB_VDDCR_SOC
AH18	VDDCR_SOC
AH19	VDDCR_SOC
AH20	VDDCR_SOC
AH21	VDDCR_SOC
AH22	VDDCR_SOC
AH23	VDDCR_SOC
AH24	VDDCR_SOC
AH25	VDDCR_SOC
AH26	VDDCR_SOC
AH27	VDDCR_SOC
AH28	VDDCR_SOC
AH29	VDDCR_SOC
AH30	VDDCR_SOC
AH31	VDDCR_SOC
AH32	VDDCR_SOC
AH33	VDDCR_SOC
AH34	VDDCR_SOC
AH35	VDDCR_SOC

Ball Reference	Signal Name
AH36	VDDCR_SOC
AH37	DFTIO_370
AH38	RSVD
AH39	VDDCR_SOC
AH40	RSVD
AH41	RSVD
AH42	RSVD
AH43	VDDCR_SOC
AH44	RSVD
AH45	VDDCR_SOC
AJ1	TX4P_DPA1P
AJ2	TX4M_DPA1N
AJ3	VSS
AJ4	RSVD
AJ5	RSVD
AJ6	VSS
AJ7	ANALOGIO
AJ8	RSVD
AJ9	VSS
AJ10	RSVD
AJ11	TEST_PG
AJ12	VSS
AJ13	VSS
AJ14	RSVD
AJ15	HBMA_DAP_49
AJ16	FB_VSS_A
AJ17	HBMA_DAP_32
AJ18	HBMA_DAP_28
AJ19	VSS
AJ20	HBMA_DAP_12
AJ21	HBMA_DAP_7
AJ22	VSS
AJ23	HBMA_DAP_17
AJ24	HBMA_DAP_8
AJ25	VSS
AJ26	HBMA_DAP_6
AJ27	HBMA_DAP_0
AJ28	VSS
AJ29	HBMB_DAP_47
AJ30	HBMB_DAP_41
AJ31	VSS
AJ32	HBMB_DAP_30

Ball Reference	Signal Name
AJ33	HBMB_DAP_24
AJ34	VSS
AJ35	HBMB_DAP_11
AJ36	HBMB_DAP_1
AJ37	VSS
AJ38	DFTIO_383
AJ39	DFTIO_378
AJ40	DFTIO_342
AJ41	VSS
AJ42	RSVD
AJ43	DFTIO_381
AJ44	RSVD
AJ45	VDDCR_SOC
AK1	VSS
AK2	TX5P_DPA0P
AK3	TX5M_DPA0N
AK4	VSS
AK5	PCIE_ZVSS
AK6	VSS
AK7	RSVD
AK8	VDD_080_EFUSE
AK9	VDD_080_EFUSE
AK10	RSVD
AK11	VSS
AK12	VSS
AK13	VSS
AK14	HBMA_DAP_59
AK15	HBMA_DAP_46
AK16	FB_VDDCI_MEM
AK17	HBMA_DAP_38
AK18	VSS
AK19	HBMA_DAP_23
AK20	HBMA_DAP_21
AK21	VSS
AK22	HBMA_DAP_14
AK23	HBMA_DAP_19
AK24	VSS
AK25	HBMA_DAP_9
AK26	HBMA_DAP_1
AK27	VSS
AK28	HBMB_DAP_59
AK29	HBMB_DAP_55

Ball Reference	Signal Name
AK30	VSS
AK31	HBMB_DAP_44
AK32	HBMB_DAP_31
AK33	VSS
AK34	HBMB_DAP_14
AK35	HBMB_DAP_10
AK36	VSS
AK37	VSS
AK38	RSVD
AK39	VSS
AK40	RSVD
AK41	DFTIO_377
AK42	DFTIO_360
AK43	VSS
AK44	DFTIO_362
AK45	VDDCR_SOC
AL1	VSS
AL2	GENERICA
AL3	VSS
AL4	GPIO_11
AL5	GPIO_12
AL6	RSVD
AL7	VDD_080
AL8	RSVD
AL9	VSS
AL10	TS_A
AL11	RSVD
AL12	VSS
AL13	VSS
AL14	HBMA_DAP_58
AL15	RSVD
AL16	VSS
AL17	VDDCI_MEM
AL18	HBMA_DAP_26
AL19	HBMA_DAP_41
AL20	VDDCI_MEM
AL21	HBMA_DAP_13
AL22	HBMA_DAP_11
AL23	VDDCI_MEM
AL24	HBMA_DAP_20
AL25	HBMA_DAP_16
AL26	VDDCI_MEM

Ball Reference	Signal Name
AL27	HBMA_DAP_5
AL28	HBMB_DAP_58
AL29	VDDCI_MEM
AL30	HBMB_DAP_50
AL31	HBMB_DAP_39
AL32	VDDCI_MEM
AL33	HBMB_DAP_21
AL34	HBMB_DAP_17
AL35	VDDCI_MEM
AL36	HBMB_DAP_7
AL37	HBMB_DAP_0
AL38	RSVD
AL39	DFTIO_382
AL40	DFTIO_371
AL41	VDDCR_SOC
AL42	DFTIO_369
AL43	DFTIO_373
AL44	DFTIO_380
AL45	VDDCR_SOC
AM1	XTALIN
AM2	VSS
AM3	XTALOUT
AM4	VSS
AM5	GPIO_14
AM6	GPIO_13
AM7	VSS
AM8	VDD_080
AM9	DBREQ_L
AM10	SDA
AM11	VSS
AM12	VSS
AM13	VSS
AM14	RSVD
AM15	MTESTA
AM16	VSS
AM17	HBMA_DAP_39
AM18	HBMA_DAP_40
AM19	VDDCI_MEM
AM20	HBMA_DAP_27
AM21	HBMA_DAP_22
AM22	VDDCI_MEM
AM23	HBMA_DAP_35

Ball Reference	Signal Name
AM24	HBMA_DAP_29
AM25	VDDCI_MEM
AM26	HBMA_DAP_4
AM27	HBMA_DAP_3
AM28	VDDCI_MEM
AM29	HBMB_DAP_48
AM30	HBMB_DAP_45
AM31	VDDCI_MEM
AM32	HBMB_DAP_27
AM33	HBMB_DAP_23
AM34	VDDCI_MEM
AM35	HBMB_DAP_13
AM36	HBMB_DAP_3
AM37	RSVD
AM38	RSVD
AM39	VDDCR_SOC
AM40	DFTIO_336
AM41	DFTIO_372
AM42	DFTIO_337
AM43	VDDCR_SOC
AM44	VDDCR_SOC
AM45	VDDCR_SOC
AN1	RSVD
AN2	RSVD
AN3	RSVD
AN4	RSVD
AN5	RSVD
AN6	RSVD
AN7	VSS
AN8	RSVD
AN9	VSS
AN10	SCL
AN11	RSVD
AN12	RSVD
AN13	VSS
AN14	RSVD
AN15	HBMA_DAP_52
AN16	VSS
AN17	HBMA_DAP_51
AN18	VSS
AN19	HBMA_DAP_50
AN20	HBMA_DAP_34

Ball Reference	Signal Name
AN21	VSS
AN22	HBMA_DAP_15
AN23	HBMA_DAP_42
AN24	VSS
AN25	HBMA_DAP_18
AN26	HBMA_DAP_10
AN27	VSS
AN28	HBMB_DAP_54
AN29	HBMB_DAP_53
AN30	VSS
AN31	HBMB_DAP_38
AN32	HBMB_DAP_33
AN33	VSS
AN34	HBMB_DAP_16
AN35	HBMB_DAP_6
AN36	VSS
AN37	MTESTB
AN38	RSVD
AN39	DFTIO_363
AN40	DFTIO_368
AN41	VSS
AN42	DFTIO_339
AN43	VDDCR_SOC
AN44	VDDCR_SOC
AN45	VDDCR_SOC
AP1	OSC_GAIN0
AP2	OSC_GAIN1
AP3	OSC_GAIN2
AP4	RSVD
AP5	RSVD
AP6	RSVD
AP7	VSS
AP8	VDD_080
AP9	RSVD
AP10	RSVD
AP11	VSS
AP12	VSS
AP13	VSS
AP14	HBMA_DAP_53
AP15	HBMA_DAP_56
AP16	VDDIO_MEM
AP17	VSS

Ball Reference	Signal Name
AP18	VDDCR_HBM
AP19	VDDCR_HBM
AP20	VSS
AP21	VDDCR_HBM
AP22	VDDCR_HBM
AP23	VSS
AP24	VDDCR_HBM
AP25	VDDCR_HBM
AP26	VSS
AP27	VDDCR_HBM
AP28	VDDCR_HBM
AP29	VSS
AP30	VDDIO_MEM
AP31	HBMB_DAP_37
AP32	VSS
AP33	VDDCR_HBM
AP34	HBMB_DAP_22
AP35	VSS
AP36	HBMB_DAP_2
AP37	HBMB_DAP_5
AP38	RSVD
AP39	DFTIO_379
AP40	DFTIO_374
AP41	DFTIO_375
AP42	VDDCR_SOC
AP43	VDDCR_SOC
AP44	VDDCR_SOC
AP45	VDDCR_SOC
AR1	BP_0
AR2	BP_1
AR3	VSS
AR4	GPIO_15
AR5	GPIO_16
AR6	GPIO_17
AR7	VSS
AR8	RSVD
AR9	VSS
AR10	RSVD
AR11	RSVD
AR12	VSS
AR13	VSS
AR14	HBMA_DAP_57

Ball Reference	Signal Name
AR15	VREFEXTA
AR16	VSS
AR17	HBMA_DAP_43
AR18	HBMA_DAP_54
AR19	VDDIO_MEM
AR20	HBMA_DAP_31
AR21	HBMA_DAP_44
AR22	VDDIO_MEM
AR23	HBMA_DAP_36
AR24	HBMA_DAP_30
AR25	VDDIO_MEM
AR26	HBMA_DAP_25
AR27	HBMA_DAP_2
AR28	VDDIO_MEM
AR29	HBMB_DAP_49
AR30	HBMB_DAP_42
AR31	VDDIO_MEM
AR32	HBMB_DAP_32
AR33	HBMB_DAP_28
AR34	VDDCR_HBM
AR35	HBMB_DAP_9
AR36	VREFEXTB
AR37	RSVD
AR38	RSVD
AR39	DFTIO_364
AR40	DFTIO_365
AR41	VDDCR_SOC
AR42	VDDCR_SOC
AR43	VDDCR_SOC
AR44	VDDCR_SOC
AR45	DFTIO_341
AT1	BP_3
AT2	BP_2
AT3	VSS
AT4	GPIO_18
AT5	GPIO_19
AT6	GPIO_20
AT7	VSS
AT8	VDD_080
AT9	RSVD
AT10	RSVD
AT11	VSS

Ball Reference	Signal Name
AT12	MACO_EN
AT13	VSS
AT14	HBMA_DAP_55
AT15	VSS
AT16	VDDCR_HBM
AT17	VDDIO_MEM
AT18	VDDIO_MEM
AT19	HBMA_DAP_48
AT20	HBMA_DAP_47
AT21	VDDIO_MEM
AT22	HBMA_DAP_45
AT23	HBMA_DAP_37
AT24	VDDIO_MEM
AT25	HBMA_DAP_33
AT26	HBMA_DAP_24
AT27	VDDIO_MEM
AT28	HBMB_DAP_57
AT29	HBMB_DAP_52
AT30	VDDIO_MEM
AT31	HBMB_DAP_43
AT32	HBMB_DAP_26
AT33	VDDIO_MEM
AT34	HBMB_DAP_18
AT35	HBMB_DAP_8
AT36	RSVD
AT37	TEMPINRETURN
AT38	VSS
AT39	VDDCR_SOC
AT40	VDDCR_SOC
AT41	VDDCR_SOC
AT42	VDDCR_SOC
AT43	DFTIO_355
AT44	DFTIO_340
AT45	DFTIO_338
AU1	RSVD
AU2	RSVD
AU3	RSVD
AU4	RSVD
AU5	RSVD
AU6	RSVD
AU7	RSVD
AU8	RSVD

Ball Reference	Signal Name
AU9	RSVD
AU10	VSS
AU11	RSVD
AU12	VSS
AU13	VSS
AU14	BL_ENABLE
AU15	RSVD
AU16	PX_EN
AU17	VSS
AU18	VDDCR_HBM
AU19	VDDIO_MEM
AU20	VSS
AU21	VDDCR_HBM
AU22	VDDCR_HBM
AU23	VSS
AU24	VDDIO_MEM
AU25	RSVD
AU26	VSS
AU27	RSVD
AU28	HBMB_DAP_56
AU29	VSS
AU30	HBMB_DAP_46
AU31	HBMB_DAP_36
AU32	VSS
AU33	HBMB_DAP_25
AU34	HBMB_DAP_12
AU35	VSS
AU36	INTCRACKMONDB
AU37	TEMPIN
AU38	VDDCR_SOC
AU39	VDDCR_SOC
AU40	VDDCR_SOC
AU41	VDDCR_SOC
AU42	DFTIO_357
AU43	DFTIO_358
AU44	DFTIO_376
AU45	VSS
AV1	RSVD
AV2	RSVD
AV3	RSVD
AV4	VDD_080
AV5	VSS

Ball Reference	Signal Name
AV6	VSS
AV7	VDD_080
AV8	RSVD
AV9	VSS
AV10	VDD_080
AV11	VSS
AV12	RSVD
AV13	RSVD
AV14	GENERICB
AV15	TEST_PG_BACO
AV16	BL_PWM_DIM
AV17	DIGON
AV18	RSVD
AV19	RSVD
AV20	RSVD
AV21	RSVD
AV22	RSVD
AV23	RSVD
AV24	VDDIO_MEM
AV25	VSS
AV26	VDDIO_MEM
AV27	VDDIO_MEM
AV28	VSS
AV29	HBMB_DAP_51
AV30	HBMB_DAP_40
AV31	VSS
AV32	HBMB_DAP_34
AV33	HBMB_DAP_19
AV34	VSS
AV35	HBMB_DAP_15
AV36	RSVD
AV37	VSS
AV38	RSVD
AV39	RSVD
AV40	DFTIO_344
AV41	DFTIO_366
AV42	DFTIO_367
AV43	VSS
AV44	DFTIO_356
AV45	RSVD
AW1	RSVD
AW2	RSVD

Ball Reference	Signal Name
AW3	VDD_080
AW4	VSS
AW5	VSS
AW6	VDD_080
AW7	RSVD
AW8	VSS
AW9	VDD_080
AW10	RSVD
AW11	VSS
AW12	RSVD
AW13	RSVD
AW14	VSS
AW15	RSVD
AW16	RSVD
AW17	VSS
AW18	VSS
AW19	VSS
AW20	VSS
AW21	VSS
AW22	VSS
AW23	RSVD
AW24	RSVD
AW25	VDDCR_HBM
AW26	RSVD
AW27	RSVD
AW28	VDDCR_HBM
AW29	RSVD
AW30	VDDIO_MEM
AW31	HBMB_DAP_35
AW32	HBMB_DAP_29
AW33	VDDIO_MEM
AW34	HBMB_DAP_20
AW35	HBMB_DAP_4
AW36	VDDIO_MEM
AW37	VDDCR_HBM
AW38	RSVD
AW39	RSVD
AW40	DFTIO_352
AW41	VSS
AW42	DFTIO_347
AW43	DFTIO_345
AW44	DFTIO_349

Ball Reference	Signal Name
AW45	VSS
AY1	PINSTRAP_7
AY2	PINSTRAP_6
AY3	PINSTRAP_5
AY4	VSS
AY5	PCIE_REFCLKP
AY6	PCIE_REFCLKN
AY7	VSS
AY8	PCIE_TX2P
AY9	PCIE_TX2N
AY10	VSS
AY11	PCIE_TX5P
AY12	PCIE_TX5N
AY13	VSS
AY14	PCIE_TX8P
AY15	PCIE_TX8N
AY16	VSS
AY17	PCIE_TX11P
AY18	PCIE_TX11N
AY19	VSS
AY20	PCIE_TX14P
AY21	PCIE_TX14N
AY22	VSS
AY23	RSVD
AY24	VDDIO_MEM
AY25	PLLCHARZ1_L
AY26	PLLCHARZ1_H
AY27	VDDCR_HBM
AY28	FB_VSS_B
AY29	FB_VDDIO_MEM_GPU
AY30	RSVD
AY31	RSVD
AY32	VDDIO_MEM
AY33	RSVD
AY34	RSVD
AY35	VDDIO_MEM
AY36	RSVD
AY37	RSVD
AY38	VDDIO_MEM
AY39	VSS
AY40	DFTIO_359
AY41	DFTIO_351

Ball Reference	Signal Name
AY42	DFTIO_346
AY43	VSS
AY44	DFTIO_353
AY45	DFTIO_343
BA2	PINSTRAP_4
BA3	PINSTRAP_3
BA4	RSVD
BA5	VSS
BA6	VSS
BA7	PCIE_TX1P
BA8	PCIE_TX1N
BA9	VSS
BA10	PCIE_TX4P
BA11	PCIE_TX4N
BA12	VSS
BA13	PCIE_TX7P
BA14	PCIE_TX7N
BA15	VSS
BA16	PCIE_TX10P
BA17	PCIE_TX10N
BA18	VSS
BA19	PCIE_TX13P
BA20	PCIE_TX13N
BA21	VSS
BA22	VSS
BA23	RSVD
BA24	RSVD
BA25	RSVD
BA26	RSVD
BA27	VSS
BA28	FB_VDDIO_MEM_HBM
BA29	FB_VDDCR_HBM
BA30	RSVD
BA31	VSS
BA32	RSVD
BA33	VDDCR_HBM
BA34	VSS
BA35	RSVD
BA36	RSVD
BA37	VSS
BA38	RSVD
BA39	RSVD

Ball Reference	Signal Name
BA40	DFTIO_354
BA41	VSS
BA42	DFTIO_361
BA43	DFTIO_348
BA44	DFTIO_350
BB1	PINSTRAP_2
BB2	PINSTRAP_1
BB3	PINSTRAP_0
BB4	VSS
BB5	VSS
BB6	PCIE_TX0P
BB7	PCIE_TX0N
BB8	VSS
BB9	PCIE_TX3P
BB10	PCIE_TX3N
BB11	VSS
BB12	PCIE_TX6P
BB13	PCIE_TX6N
BB14	VSS
BB15	PCIE_TX9P
BB16	PCIE_TX9N
BB17	VSS
BB18	PCIE_TX12P
BB19	PCIE_TX12N
BB20	VSS
BB21	PCIE_TX15P
BB22	PCIE_TX15N
BB23	VSS
BB24	RSVD
BB25	RSVD
BB26	RSVD
BB27	RSVD
BB28	VSS
BB29	VSS
BB30	VSS
BB31	RSVD
BB32	RSVD
BB33	VDDIO_MEM
BB34	DPLUS
BB35	VDDIO_MEM
BB36	VDDIO_MEM
BB37	RSVD

Ball Reference	Signal Name
BB38	RSVD
BB39	VDDIO_MEM
BB40	RSVD
BB41	RSVD
BB42	VSS
BB43	RSVD
BB44	VSS
BB45	VSS
BC1	SMBDAT
BC2	SMBCLK
BC3	RSVD
BC4	VSS
BC5	PCIE_RX0P
BC6	PCIE_RX0N
BC7	VSS
BC8	PCIE_RX3P
BC9	PCIE_RX3N
BC10	VSS
BC11	PCIE_RX6P
BC12	PCIE_RX6N
BC13	VSS
BC14	PCIE_RX9P
BC15	PCIE_RX9N
BC16	VSS
BC17	PCIE_RX12P
BC18	PCIE_RX12N
BC19	VSS
BC20	PCIE_RX15P
BC21	PCIE_RX15N
BC22	VSS
BC23	RSVD
BC24	RSVD
BC25	VSS
BC26	RSVD
BC27	RSVD
BC28	RSVD
BC29	PROCHOT_L
BC30	VSS
BC31	RSVD
BC32	VSS
BC33	RSVD
BC34	DMINUS

Ball Reference	Signal Name
BC35	VSS
BC36	RSVD
BC37	RSVD
BC38	VSS
BC39	RSVD
BC40	RSVD
BC41	VSS
BC42	INTCRACKMONPDG
BC43	INTCRACKMONP
BC44	VSS
BC45	VSS
BD1	VSS
BD2	WAKEB
BD3	PERSTB
BD4	RSVD
BD5	VSS
BD6	VSS
BD7	PCIE_RX2P
BD8	PCIE_RX2N
BD9	VSS
BD10	PCIE_RX5P
BD11	PCIE_RX5N
BD12	VSS
BD13	PCIE_RX8P
BD14	PCIE_RX8N
BD15	VSS
BD16	PCIE_RX11P
BD17	PCIE_RX11N
BD18	VSS
BD19	PCIE_RX14P
BD20	PCIE_RX14N
BD21	VSS
BD22	RSVD
BD23	VSS
BD24	RSVD
BD25	VSS
BD26	VPP
BD27	RSVD
BD28	RSVD
BD29	FANOUT
BD30	DDCVGACLK
BD31	ALERT_L

Ball Reference	Signal Name
BD32	RSVD
BD33	PUMPOUT
BD34	VSS
BD35	RSVD
BD36	RSVD
BD37	VSS
BD38	RSVD
BD39	RSVD
BD40	VSS
BD41	RSVD
BD42	RSVD
BD43	VSS
BD44	VSS
BD45	VSS
BE2	VSS
BE3	CLKREQB
BE4	VSS
BE6	PCIE_RX1P
BE7	PCIE_RX1N
BE8	VSS
BE9	PCIE_RX4P
BE10	PCIE_RX4N
BE11	VSS
BE12	PCIE_RX7P
BE13	PCIE_RX7N
BE14	VSS
BE15	PCIE_RX10P
BE16	PCIE_RX10N
BE17	VSS
BE18	PCIE_RX13P
BE19	PCIE_RX13N
BE20	VSS
BE21	VSS
BE22	REFCLKP
BE23	REFCLKN
BE24	RSVD
BE25	VSS
BE26	VPP
BE27	VPP
BE28	VSS
BE29	FANIN
BE30	DDCVGADATA

Ball Reference	Signal Name
BE31	CTF
BE32	RSVD
BE33	PUMPIN
BE34	VSS
BE35	RSVD
BE36	RSVD
BE37	VSS
BE38	RSVD
BE39	VSS
BE40	RSVD
BE42	VSS
BE43	VSS
BE44	VSS

A.2 Pins Sorted by Signal Name

Table A–2 Pins Sorted by Signal Name

Signal Name	Ball Reference
ALERT_L	BD31
ANALOGIO	AJ7
AUX1N	G5
AUX1P	G4
AUX2N	K3
AUX2P	K2
AUX_ZVSS	P5
BL_ENABLE	AU14
BL_PWM_DIM	AV16
BP_0	AR1
BP_1	AR2
BP_2	AT2
BP_3	AT1
CLKREQB	BE3
CTF	BE31
DBREQ_L	AM9
DDC1CLK	F6
DDC1DATA	F5
DDC2CLK	J5
DDC2DATA	J4
DDCAUX3N	R5
DDCAUX3P	R4
DDCAUX4N	W5

Signal Name	Ball Reference
DDCAUX4P	W4
DDCAUX5N	AD6
DDCAUX5P	AD5
DDCAUX6N	AF6
DDCAUX6P	AF5
DDCVGACLK	BD30
DDCVGADATA	BE30
DFTIO_0	J7
DFTIO_1	L11
DFTIO_2	E4
DFTIO_3	L8
DFTIO_4	M10
DFTIO_5	E3
DFTIO_6	M9
DFTIO_7	L7
DFTIO_8	N8
DFTIO_9	C2
DFTIO_10	N10
DFTIO_11	M8
DFTIO_12	E6
DFTIO_13	D4
DFTIO_14	K9
DFTIO_15	P9
DFTIO_16	E7
DFTIO_17	C1
DFTIO_18	D2
DFTIO_19	K10
DFTIO_20	H8
DFTIO_21	C3
DFTIO_22	C4
DFTIO_23	K8
DFTIO_24	L10
DFTIO_25	F8
DFTIO_26	J8
DFTIO_27	D3
DFTIO_28	G8
DFTIO_29	B2
DFTIO_30	H10
DFTIO_31	B5
DFTIO_32	C6
DFTIO_33	D5
DFTIO_34	E8

Signal Name	Ball Reference
DFTIO_35	J10
DFTIO_36	D8
DFTIO_37	J11
DFTIO_38	F10
DFTIO_39	D6
DFTIO_40	J14
DFTIO_41	J12
DFTIO_42	G10
DFTIO_43	H9
DFTIO_44	B4
DFTIO_45	G12
DFTIO_46	F12
DFTIO_47	D9
DFTIO_48	B6
DFTIO_49	C7
DFTIO_50	F13
DFTIO_51	J16
DFTIO_52	C8
DFTIO_53	F9
DFTIO_54	J15
DFTIO_55	E12
DFTIO_56	E11
DFTIO_57	G11
DFTIO_58	B8
DFTIO_59	H12
DFTIO_60	H16
DFTIO_61	F14
DFTIO_62	E14
DFTIO_63	G14
DFTIO_64	E10
DFTIO_65	D13
DFTIO_66	H20
DFTIO_67	H18
DFTIO_68	B9
DFTIO_69	H13
DFTIO_70	D10
DFTIO_71	H17
DFTIO_72	H21
DFTIO_73	H14
DFTIO_74	C14
DFTIO_75	C10
DFTIO_76	G18

Signal Name	Ball Reference
DFTIO_77	D14
DFTIO_78	H22
DFTIO_79	E15
DFTIO_80	G16
DFTIO_81	G22
DFTIO_82	C15
DFTIO_83	G15
DFTIO_84	E16
DFTIO_85	C16
DFTIO_86	B13
DFTIO_87	C11
DFTIO_88	G19
DFTIO_89	F16
DFTIO_90	J18
DFTIO_91	B14
DFTIO_92	D16
DFTIO_93	G24
DFTIO_94	E18
DFTIO_95	F17
DFTIO_96	C18
DFTIO_97	B16
DFTIO_98	G20
DFTIO_99	J20
DFTIO_100	J19
DFTIO_101	D17
DFTIO_102	C19
DFTIO_103	F18
DFTIO_104	C20
DFTIO_105	D18
DFTIO_106	E22
DFTIO_107	B17
DFTIO_108	D20
DFTIO_109	B18
DFTIO_110	D21
DFTIO_111	E19
DFTIO_112	B20
DFTIO_113	H26
DFTIO_114	G23
DFTIO_115	C22
DFTIO_116	D22
DFTIO_117	E20
DFTIO_118	C26

Signal Name	Ball Reference
DFTIO_119	C23
DFTIO_120	B21
DFTIO_121	B22
DFTIO_122	F22
DFTIO_123	G26
DFTIO_124	J26
DFTIO_125	J22
DFTIO_126	E23
DFTIO_127	F20
DFTIO_128	D24
DFTIO_129	C24
DFTIO_130	G28
DFTIO_131	C27
DFTIO_132	D25
DFTIO_133	C31
DFTIO_134	F25
DFTIO_135	B24
DFTIO_136	B25
DFTIO_137	D28
DFTIO_138	F21
DFTIO_139	C28
DFTIO_140	J27
DFTIO_141	E24
DFTIO_142	D29
DFTIO_143	B26
DFTIO_144	G27
DFTIO_145	F24
DFTIO_146	D26
DFTIO_147	C32
DFTIO_148	E30
DFTIO_149	D36
DFTIO_150	J23
DFTIO_151	C34
DFTIO_152	B28
DFTIO_153	C30
DFTIO_154	D30
DFTIO_155	H24
DFTIO_156	G31
DFTIO_157	E28
DFTIO_158	B29
DFTIO_159	F26
DFTIO_160	J24

Signal Name	Ball Reference
DFTIO_161	B30
DFTIO_162	D32
DFTIO_163	E31
DFTIO_164	D38
DFTIO_165	B32
DFTIO_166	B33
DFTIO_167	C35
DFTIO_168	F28
DFTIO_169	C38
DFTIO_170	H25
DFTIO_171	G30
DFTIO_172	D40
DFTIO_173	E32
DFTIO_174	B34
DFTIO_175	C36
DFTIO_176	E26
DFTIO_177	E27
DFTIO_178	H28
DFTIO_179	D33
DFTIO_180	D42
DFTIO_181	D37
DFTIO_182	C43
DFTIO_183	F29
DFTIO_184	J28
DFTIO_185	F32
DFTIO_186	D44
DFTIO_187	B44
DFTIO_188	E44
DFTIO_189	C44
DFTIO_190	D34
DFTIO_191	H29
DFTIO_192	D41
DFTIO_193	J35
DFTIO_194	E42
DFTIO_195	F42
DFTIO_196	F30
DFTIO_197	J30
DFTIO_198	H30
DFTIO_199	E43
DFTIO_200	F40
DFTIO_201	B40
DFTIO_202	B41

Signal Name	Ball Reference
DFTIO_203	B38
DFTIO_204	C42
DFTIO_205	G44
DFTIO_206	F34
DFTIO_207	H37
DFTIO_208	E34
DFTIO_209	B42
DFTIO_210	B36
DFTIO_211	B37
DFTIO_212	G32
DFTIO_213	J31
DFTIO_214	E35
DFTIO_215	F44
DFTIO_216	E39
DFTIO_217	C40
DFTIO_218	H36
DFTIO_219	E38
DFTIO_220	F33
DFTIO_221	E36
DFTIO_222	C39
DFTIO_223	G42
DFTIO_224	G43
DFTIO_225	H44
DFTIO_226	H42
DFTIO_227	G36
DFTIO_228	E40
DFTIO_229	F41
DFTIO_230	J43
DFTIO_231	J44
DFTIO_232	J32
DFTIO_233	K44
DFTIO_234	G35
DFTIO_235	F38
DFTIO_236	M44
DFTIO_237	L44
DFTIO_238	H34
DFTIO_239	K41
DFTIO_240	L43
DFTIO_241	K42
DFTIO_242	J42
DFTIO_243	F37
DFTIO_244	G40

Signal Name	Ball Reference
DFTIO_245	G39
DFTIO_246	K40
DFTIO_247	J34
DFTIO_248	L42
DFTIO_249	H41
DFTIO_250	N43
DFTIO_251	N44
DFTIO_252	G34
DFTIO_253	M42
DFTIO_254	F36
DFTIO_255	J36
DFTIO_256	J39
DFTIO_257	G38
DFTIO_258	P44
DFTIO_259	J40
DFTIO_260	N42
DFTIO_261	M41
DFTIO_262	R43
DFTIO_263	R44
DFTIO_264	J38
DFTIO_265	K37
DFTIO_266	V44
DFTIO_267	P42
DFTIO_268	T42
DFTIO_269	H38
DFTIO_270	R39
DFTIO_271	U42
DFTIO_272	H40
DFTIO_273	V41
DFTIO_274	V42
DFTIO_275	M37
DFTIO_276	L40
DFTIO_277	T41
DFTIO_278	U38
DFTIO_279	U39
DFTIO_280	L38
DFTIO_281	H33
DFTIO_282	M40
DFTIO_283	V38
DFTIO_284	R42
DFTIO_285	T44
DFTIO_286	K38

Signal Name	Ball Reference
DFTIO_287	N40
DFTIO_288	P41
DFTIO_289	L39
DFTIO_290	H32
DFTIO_291	W38
DFTIO_292	W39
DFTIO_293	W40
DFTIO_294	Y38
DFTIO_295	P37
DFTIO_296	U44
DFTIO_297	W44
DFTIO_298	U43
DFTIO_299	V40
DFTIO_300	N39
DFTIO_301	P40
DFTIO_302	Y44
DFTIO_303	T40
DFTIO_304	W42
DFTIO_305	Y42
DFTIO_306	W43
DFTIO_307	AA44
DFTIO_308	U40
DFTIO_309	R40
DFTIO_310	M38
DFTIO_311	AB44
DFTIO_312	AA42
DFTIO_313	AA43
DFTIO_314	AB41
DFTIO_315	R38
DFTIO_316	Y40
DFTIO_317	AB40
DFTIO_318	AA39
DFTIO_319	AC40
DFTIO_320	N38
DFTIO_321	AA40
DFTIO_322	T38
DFTIO_323	Y41
DFTIO_324	P38
DFTIO_325	AB42
DFTIO_326	AC39
DFTIO_327	AD41
DFTIO_328	AC44

Signal Name	Ball Reference
DFTIO_329	AA38
DFTIO_330	AC43
DFTIO_331	AD42
DFTIO_332	AB37
DFTIO_333	AC42
DFTIO_334	AC38
DFTIO_335	AB38
DFTIO_336	AM40
DFTIO_337	AM42
DFTIO_338	AT45
DFTIO_339	AN42
DFTIO_340	AT44
DFTIO_341	AR45
DFTIO_342	AJ40
DFTIO_343	AY45
DFTIO_344	AV40
DFTIO_345	AW43
DFTIO_346	AY42
DFTIO_347	AW42
DFTIO_348	BA43
DFTIO_349	AW44
DFTIO_350	BA44
DFTIO_351	AY41
DFTIO_352	AW40
DFTIO_353	AY44
DFTIO_354	BA40
DFTIO_355	AT43
DFTIO_356	AV44
DFTIO_357	AU42
DFTIO_358	AU43
DFTIO_359	AY40
DFTIO_360	AK42
DFTIO_361	BA42
DFTIO_362	AK44
DFTIO_363	AN39
DFTIO_364	AR39
DFTIO_365	AR40
DFTIO_366	AV41
DFTIO_367	AV42
DFTIO_368	AN40
DFTIO_369	AL42
DFTIO_370	AH37

Signal Name	Ball Reference
DFTIO_371	AL40
DFTIO_372	AM41
DFTIO_373	AL43
DFTIO_374	AP40
DFTIO_375	AP41
DFTIO_376	AU44
DFTIO_377	AK41
DFTIO_378	AJ39
DFTIO_379	AP39
DFTIO_380	AL44
DFTIO_381	AJ43
DFTIO_382	AL39
DFTIO_383	AJ38
DIGON	AV17
DMINUS	BC34
DPLUS	BB34
DP_ZVDD_08	AH6
DP_ZVSS	AG6
FANIN	BE29
FANOUT	BD29
FB_VDDCI_MEM	AK16
FB_VDDCR_HBM	BA29
FB_VDDCR_SOC	AH17
FB_VDDIO_MEM_GPU	AY29
FB_VDDIO_MEM_HBM	BA28
FB_VSS_A	AJ16
FB_VSS_B	AY28
GENERICA	AL2
GENERICB	AV14
GENERICC_HPD2	K5
GENERICD_HPD3	P6
GENERICE_HPD4	V5
GENERICF_HPD5	AC4
GENERICG_HPD6	AE4
GENLK_CLK	R7
GENLK_VSYNC	R8
GPIO_0	T8
GPIO_1	U7
GPIO_2	V7
GPIO_3	AG8
GPIO_4	AG7
GPIO_5	AE7

Signal Name	Ball Reference
GPIO_6	AE8
GPIO_7_ROMSCK	W7
GPIO_8_ROMSI	W8
GPIO_9_ROMSO	V6
GPIO_10_ROMCSB	Y7
GPIO_11	AL4
GPIO_12	AL5
GPIO_13	AM6
GPIO_14	AM5
GPIO_15	AR4
GPIO_16	AR5
GPIO_17	AR6
GPIO_18	AT4
GPIO_19	AT5
GPIO_20	AT6
GPIO_SVC0	V9
GPIO_SVD0	T9
GPIO_SVT0	U8
HBMA_DAP_0	AJ27
HBMA_DAP_1	AK26
HBMA_DAP_2	AR27
HBMA_DAP_3	AM27
HBMA_DAP_4	AM26
HBMA_DAP_5	AL27
HBMA_DAP_6	AJ26
HBMA_DAP_7	AJ21
HBMA_DAP_8	AJ24
HBMA_DAP_9	AK25
HBMA_DAP_10	AN26
HBMA_DAP_11	AL22
HBMA_DAP_12	AJ20
HBMA_DAP_13	AL21
HBMA_DAP_14	AK22
HBMA_DAP_15	AN22
HBMA_DAP_16	AL25
HBMA_DAP_17	AJ23
HBMA_DAP_18	AN25
HBMA_DAP_19	AK23
HBMA_DAP_20	AL24
HBMA_DAP_21	AK20
HBMA_DAP_22	AM21
HBMA_DAP_23	AK19

Signal Name	Ball Reference
HBMA_DAP_24	AT26
HBMA_DAP_25	AR26
HBMA_DAP_26	AL18
HBMA_DAP_27	AM20
HBMA_DAP_28	AJ18
HBMA_DAP_29	AM24
HBMA_DAP_30	AR24
HBMA_DAP_31	AR20
HBMA_DAP_32	AJ17
HBMA_DAP_33	AT25
HBMA_DAP_34	AN20
HBMA_DAP_35	AM23
HBMA_DAP_36	AR23
HBMA_DAP_37	AT23
HBMA_DAP_38	AK17
HBMA_DAP_39	AM17
HBMA_DAP_40	AM18
HBMA_DAP_41	AL19
HBMA_DAP_42	AN23
HBMA_DAP_43	AR17
HBMA_DAP_44	AR21
HBMA_DAP_45	AT22
HBMA_DAP_46	AK15
HBMA_DAP_47	AT20
HBMA_DAP_48	AT19
HBMA_DAP_49	AJ15
HBMA_DAP_50	AN19
HBMA_DAP_51	AN17
HBMA_DAP_52	AN15
HBMA_DAP_53	AP14
HBMA_DAP_54	AR18
HBMA_DAP_55	AT14
HBMA_DAP_56	AP15
HBMA_DAP_57	AR14
HBMA_DAP_58	AL14
HBMA_DAP_59	AK14
HBMB_DAP_0	AL37
HBMB_DAP_1	AJ36
HBMB_DAP_2	AP36
HBMB_DAP_3	AM36
HBMB_DAP_4	AW35
HBMB_DAP_5	AP37

Signal Name	Ball Reference
HBMB_DAP_6	AN35
HBMB_DAP_7	AL36
HBMB_DAP_8	AT35
HBMB_DAP_9	AR35
HBMB_DAP_10	AK35
HBMB_DAP_11	AJ35
HBMB_DAP_12	AU34
HBMB_DAP_13	AM35
HBMB_DAP_14	AK34
HBMB_DAP_15	AV35
HBMB_DAP_16	AN34
HBMB_DAP_17	AL34
HBMB_DAP_18	AT34
HBMB_DAP_19	AV33
HBMB_DAP_20	AW34
HBMB_DAP_21	AL33
HBMB_DAP_22	AP34
HBMB_DAP_23	AM33
HBMB_DAP_24	AJ33
HBMB_DAP_25	AU33
HBMB_DAP_26	AT32
HBMB_DAP_27	AM32
HBMB_DAP_28	AR33
HBMB_DAP_29	AW32
HBMB_DAP_30	AJ32
HBMB_DAP_31	AK32
HBMB_DAP_32	AR32
HBMB_DAP_33	AN32
HBMB_DAP_34	AV32
HBMB_DAP_35	AW31
HBMB_DAP_36	AU31
HBMB_DAP_37	AP31
HBMB_DAP_38	AN31
HBMB_DAP_39	AL31
HBMB_DAP_40	AV30
HBMB_DAP_41	AJ30
HBMB_DAP_42	AR30
HBMB_DAP_43	AT31
HBMB_DAP_44	AK31
HBMB_DAP_45	AM30
HBMB_DAP_46	AU30
HBMB_DAP_47	AJ29

Signal Name	Ball Reference
HBMB_DAP_48	AM29
HBMB_DAP_49	AR29
HBMB_DAP_50	AL30
HBMB_DAP_51	AV29
HBMB_DAP_52	AT29
HBMB_DAP_53	AN29
HBMB_DAP_54	AN28
HBMB_DAP_55	AK29
HBMB_DAP_56	AU28
HBMB_DAP_57	AT28
HBMB_DAP_58	AL28
HBMB_DAP_59	AK28
HPD1	G7
INTCRACKMONDA	AE10
INTCRACKMONDB	AU36
INTCRACKMONGLL	V10
INTCRACKMONGLR	Y10
INTCRACKMONGUL	V37
INTCRACKMONGUR	Y37
INTCRACKMONP	BC43
INTCRACKMONPDG	BC42
MACO_EN	AT12
MTESTA	AM15
MTESTB	AN37
OSC_GAIN0	AP1
OSC_GAIN1	AP2
OSC_GAIN2	AP3
PCIE_REFCLKN	AY6
PCIE_REFCLKP	AY5
PCIE_RX0N	BC6
PCIE_RX0P	BC5
PCIE_RX1N	BE7
PCIE_RX1P	BE6
PCIE_RX2N	BD8
PCIE_RX2P	BD7
PCIE_RX3N	BC9
PCIE_RX3P	BC8
PCIE_RX4N	BE10
PCIE_RX4P	BE9
PCIE_RX5N	BD11
PCIE_RX5P	BD10
PCIE_RX6N	BC12

Signal Name	Ball Reference
PCIE_RX6P	BC11
PCIE_RX7N	BE13
PCIE_RX7P	BE12
PCIE_RX8N	BD14
PCIE_RX8P	BD13
PCIE_RX9N	BC15
PCIE_RX9P	BC14
PCIE_RX10N	BE16
PCIE_RX10P	BE15
PCIE_RX11N	BD17
PCIE_RX11P	BD16
PCIE_RX12N	BC18
PCIE_RX12P	BC17
PCIE_RX13N	BE19
PCIE_RX13P	BE18
PCIE_RX14N	BD20
PCIE_RX14P	BD19
PCIE_RX15N	BC21
PCIE_RX15P	BC20
PCIE_TX0N	BB7
PCIE_TX0P	BB6
PCIE_TX1N	BA8
PCIE_TX1P	BA7
PCIE_TX2N	AY9
PCIE_TX2P	AY8
PCIE_TX3N	BB10
PCIE_TX3P	BB9
PCIE_TX4N	BA11
PCIE_TX4P	BA10
PCIE_TX5N	AY12
PCIE_TX5P	AY11
PCIE_TX6N	BB13
PCIE_TX6P	BB12
PCIE_TX7N	BA14
PCIE_TX7P	BA13
PCIE_TX8N	AY15
PCIE_TX8P	AY14
PCIE_TX9N	BB16
PCIE_TX9P	BB15
PCIE_TX10N	BA17
PCIE_TX10P	BA16
PCIE_TX11N	AY18

Signal Name	Ball Reference
PCIE_TX11P	AY17
PCIE_TX12N	BB19
PCIE_TX12P	BB18
PCIE_TX13N	BA20
PCIE_TX13P	BA19
PCIE_TX14N	AY21
PCIE_TX14P	AY20
PCIE_TX15N	BB22
PCIE_TX15P	BB21
PCIE_ZVSS	AK5
PERSTB	BD3
PINSTRAP_0	BB3
PINSTRAP_1	BB2
PINSTRAP_2	BB1
PINSTRAP_3	BA3
PINSTRAP_4	BA2
PINSTRAP_5	AY3
PINSTRAP_6	AY2
PINSTRAP_7	AY1
PLLCHARZ1_H	AY26
PLLCHARZ1_L	AY25
PROCHOT_L	BC29
PUMPIN	BE33
PUMPOUT	BD33
PX_EN	AU16
REFCLKN	BE23
REFCLKP	BE22
RSVD	B1
RSVD	B12
RSVD	C12
RSVD	D12
RSVD	L4
RSVD	N7
RSVD	N11
RSVD	P8
RSVD	P10
RSVD	R10
RSVD	R11
RSVD	T10
RSVD	U4
RSVD	U5
RSVD	U10

Signal Name	Ball Reference
RSVD	U11
RSVD	W10
RSVD	W11
RSVD	Y9
RSVD	AA4
RSVD	AA7
RSVD	AA10
RSVD	AA11
RSVD	AB10
RSVD	AC10
RSVD	AC11
RSVD	AD10
RSVD	AD37
RSVD	AD38
RSVD	AD40
RSVD	AD44
RSVD	AE11
RSVD	AE38
RSVD	AE39
RSVD	AE40
RSVD	AE42
RSVD	AE43
RSVD	AE44
RSVD	AF10
RSVD	AF37
RSVD	AF38
RSVD	AF40
RSVD	AF41
RSVD	AF42
RSVD	AF44
RSVD	AG38
RSVD	AG39
RSVD	AG40
RSVD	AG42
RSVD	AG43
RSVD	AG44
RSVD	AH38
RSVD	AH40
RSVD	AH41
RSVD	AH42
RSVD	AH44
RSVD	AJ4

Signal Name	Ball Reference
RSVD	AJ5
RSVD	AJ8
RSVD	AJ10
RSVD	AJ14
RSVD	AJ42
RSVD	AJ44
RSVD	AK7
RSVD	AK10
RSVD	AK38
RSVD	AK40
RSVD	AL6
RSVD	AL8
RSVD	AL11
RSVD	AL15
RSVD	AL38
RSVD	AM14
RSVD	AM37
RSVD	AM38
RSVD	AN1
RSVD	AN2
RSVD	AN3
RSVD	AN4
RSVD	AN5
RSVD	AN6
RSVD	AN8
RSVD	AN11
RSVD	AN12
RSVD	AN14
RSVD	AN38
RSVD	AP4
RSVD	AP5
RSVD	AP6
RSVD	AP9
RSVD	AP10
RSVD	AP38
RSVD	AR8
RSVD	AR10
RSVD	AR11
RSVD	AR37
RSVD	AR38
RSVD	AT9
RSVD	AT10

Signal Name	Ball Reference
RSVD	AT36
RSVD	AU1
RSVD	AU2
RSVD	AU3
RSVD	AU4
RSVD	AU5
RSVD	AU6
RSVD	AU7
RSVD	AU8
RSVD	AU9
RSVD	AU11
RSVD	AU15
RSVD	AU25
RSVD	AU27
RSVD	AV1
RSVD	AV2
RSVD	AV3
RSVD	AV8
RSVD	AV12
RSVD	AV13
RSVD	AV18
RSVD	AV19
RSVD	AV20
RSVD	AV21
RSVD	AV22
RSVD	AV23
RSVD	AV36
RSVD	AV38
RSVD	AV39
RSVD	AV45
RSVD	AW1
RSVD	AW2
RSVD	AW7
RSVD	AW10
RSVD	AW12
RSVD	AW13
RSVD	AW15
RSVD	AW16
RSVD	AW23
RSVD	AW24
RSVD	AW26
RSVD	AW27

Signal Name	Ball Reference
RSVD	AW29
RSVD	AW38
RSVD	AW39
RSVD	AY23
RSVD	AY30
RSVD	AY31
RSVD	AY33
RSVD	AY34
RSVD	AY36
RSVD	AY37
RSVD	BA4
RSVD	BA23
RSVD	BA24
RSVD	BA25
RSVD	BA26
RSVD	BA30
RSVD	BA32
RSVD	BA35
RSVD	BA36
RSVD	BA38
RSVD	BA39
RSVD	BB24
RSVD	BB25
RSVD	BB26
RSVD	BB27
RSVD	BB31
RSVD	BB32
RSVD	BB37
RSVD	BB38
RSVD	BB40
RSVD	BB41
RSVD	BB43
RSVD	BC3
RSVD	BC23
RSVD	BC24
RSVD	BC26
RSVD	BC27
RSVD	BC28
RSVD	BC31
RSVD	BC33
RSVD	BC36
RSVD	BC37

Signal Name	Ball Reference
RSVD	BC39
RSVD	BC40
RSVD	BD4
RSVD	BD22
RSVD	BD24
RSVD	BD27
RSVD	BD28
RSVD	BD32
RSVD	BD35
RSVD	BD36
RSVD	BD38
RSVD	BD39
RSVD	BD41
RSVD	BD42
RSVD	BE24
RSVD	BE32
RSVD	BE35
RSVD	BE36
RSVD	BE38
RSVD	BE40
SCL	AN10
SDA	AM10
SMBCLK	BC2
SMBDAT	BC1
SWAPLOCKA	T5
SWAPLOCKB	T6
TCK	AC8
TDI	AB9
TDO	AB8
TEMPIN	AU37
TEMPINRETURN	AT37
TEST6	T37
TESTEN	AD8
TEST_PG	AJ11
TEST_PG_BACO	AV15
TMS	AC7
TRST_L	AA8
TS_A	AL10
TX0M_DPB2N	AD3
TX0M_DPD2N	T3
TX0M_DPF2N	G2
TX0P_DPB2P	AD2

Signal Name	Ball Reference
TX0P_DPD2P	T2
TX0P_DPF2P	G1
TX1M_DPB1N	AE2
TX1M_DPD1N	U2
TX1M_DPF1N	H3
TX1P_DPB1P	AE1
TX1P_DPD1P	U1
TX1P_DPF1P	H2
TX2M_DPB0N	AF3
TX2M_DPD0N	V3
TX2M_DPF0N	J2
TX2P_DPB0P	AF2
TX2P_DPD0P	V2
TX2P_DPF0P	J1
TX3M_DPA2N	AH3
TX3M_DPC2N	Y3
TX3M_DPE2N	M3
TX3P_DPA2P	AH2
TX3P_DPC2P	Y2
TX3P_DPE2P	M2
TX4M_DPA1N	AJ2
TX4M_DPC1N	AA2
TX4M_DPE1N	N2
TX4P_DPA1P	AJ1
TX4P_DPC1P	AA1
TX4P_DPE1P	N1
TX5M_DPA0N	AK3
TX5M_DPC0N	AB3
TX5M_DPE0N	P3
TX5P_DPA0P	AK2
TX5P_DPC0P	AB2
TX5P_DPE0P	P2
TXCAM_DPA3N	AG2
TXCAP_DPA3P	AG1
TXCBM_DPB3N	AC2
TXCBP_DPB3P	AC1
TXCCM_DPC3N	W2
TXCCP_DPC3P	W1
TXCDM_DPD3N	R2
TXCDP_DPD3P	R1
TXCEM_DPE3N	L2
TXCEP_DPE3P	L1

Signal Name	Ball Reference
TXCFM_DPF3N	F3
TXCFP_DPF3P	F2
VDDAN_18	M5
VDDAN_18	M6
VDDAN_18	N4
VDDAN_18	N6
VDDAN_33	H5
VDDAN_33	H6
VDDAN_33	K6
VDDAN_33	L6
VDDAN_Q_EFUSE	AF8
VDDAN_Q_EFUSE	AF9
VDDCI_MEM	AL17
VDDCI_MEM	AL20
VDDCI_MEM	AL23
VDDCI_MEM	AL26
VDDCI_MEM	AL29
VDDCI_MEM	AL32
VDDCI_MEM	AL35
VDDCI_MEM	AM19
VDDCI_MEM	AM22
VDDCI_MEM	AM25
VDDCI_MEM	AM28
VDDCI_MEM	AM31
VDDCI_MEM	AM34
VDDCR_BACO	AG10
VDDCR_BACO	AG11
VDDCR_BACO	AH9
VDDCR_BACO	AH10
VDDCR_HBM	AP18
VDDCR_HBM	AP19
VDDCR_HBM	AP21
VDDCR_HBM	AP22
VDDCR_HBM	AP24
VDDCR_HBM	AP25
VDDCR_HBM	AP27
VDDCR_HBM	AP28
VDDCR_HBM	AP33
VDDCR_HBM	AR34
VDDCR_HBM	AT16
VDDCR_HBM	AU18
VDDCR_HBM	AU21

Signal Name	Ball Reference
VDDCR_HBM	AU22
VDDCR_HBM	AW25
VDDCR_HBM	AW28
VDDCR_HBM	AW37
VDDCR_HBM	AY27
VDDCR_HBM	BA33
VDDCR_SOC	A2
VDDCR_SOC	A3
VDDCR_SOC	A4
VDDCR_SOC	A6
VDDCR_SOC	A7
VDDCR_SOC	A8
VDDCR_SOC	A9
VDDCR_SOC	A10
VDDCR_SOC	A11
VDDCR_SOC	A12
VDDCR_SOC	A13
VDDCR_SOC	A14
VDDCR_SOC	A15
VDDCR_SOC	A16
VDDCR_SOC	A17
VDDCR_SOC	A18
VDDCR_SOC	A19
VDDCR_SOC	A20
VDDCR_SOC	A21
VDDCR_SOC	A22
VDDCR_SOC	A23
VDDCR_SOC	A24
VDDCR_SOC	A25
VDDCR_SOC	A26
VDDCR_SOC	A27
VDDCR_SOC	A28
VDDCR_SOC	A29
VDDCR_SOC	A30
VDDCR_SOC	A31
VDDCR_SOC	A32
VDDCR_SOC	A33
VDDCR_SOC	A34
VDDCR_SOC	A35
VDDCR_SOC	A36
VDDCR_SOC	A37
VDDCR_SOC	A38

Signal Name	Ball Reference
VDDCR_SOC	A39
VDDCR_SOC	A40
VDDCR_SOC	A42
VDDCR_SOC	A43
VDDCR_SOC	A44
VDDCR_SOC	B10
VDDCR_SOC	B15
VDDCR_SOC	B19
VDDCR_SOC	B23
VDDCR_SOC	B27
VDDCR_SOC	B31
VDDCR_SOC	B35
VDDCR_SOC	B45
VDDCR_SOC	C45
VDDCR_SOC	D15
VDDCR_SOC	D19
VDDCR_SOC	D23
VDDCR_SOC	D27
VDDCR_SOC	D31
VDDCR_SOC	D35
VDDCR_SOC	D45
VDDCR_SOC	F15
VDDCR_SOC	F19
VDDCR_SOC	F23
VDDCR_SOC	F27
VDDCR_SOC	F31
VDDCR_SOC	F35
VDDCR_SOC	F45
VDDCR_SOC	G45
VDDCR_SOC	H15
VDDCR_SOC	H19
VDDCR_SOC	H23
VDDCR_SOC	H27
VDDCR_SOC	H31
VDDCR_SOC	H35
VDDCR_SOC	H39
VDDCR_SOC	H43
VDDCR_SOC	H45
VDDCR_SOC	J13
VDDCR_SOC	J17
VDDCR_SOC	J21
VDDCR_SOC	J25

Signal Name	Ball Reference
VDDCR_SOC	J29
VDDCR_SOC	J33
VDDCR_SOC	J45
VDDCR_SOC	K13
VDDCR_SOC	K14
VDDCR_SOC	K17
VDDCR_SOC	K18
VDDCR_SOC	K21
VDDCR_SOC	K22
VDDCR_SOC	K25
VDDCR_SOC	K26
VDDCR_SOC	K29
VDDCR_SOC	K30
VDDCR_SOC	K33
VDDCR_SOC	K34
VDDCR_SOC	K39
VDDCR_SOC	K43
VDDCR_SOC	K45
VDDCR_SOC	L13
VDDCR_SOC	L14
VDDCR_SOC	L17
VDDCR_SOC	L18
VDDCR_SOC	L21
VDDCR_SOC	L22
VDDCR_SOC	L25
VDDCR_SOC	L26
VDDCR_SOC	L29
VDDCR_SOC	L30
VDDCR_SOC	L33
VDDCR_SOC	L34
VDDCR_SOC	L35
VDDCR_SOC	L36
VDDCR_SOC	L37
VDDCR_SOC	L41
VDDCR_SOC	L45
VDDCR_SOC	M13
VDDCR_SOC	M14
VDDCR_SOC	M17
VDDCR_SOC	M18
VDDCR_SOC	M21
VDDCR_SOC	M22
VDDCR_SOC	M25

Signal Name	Ball Reference
VDDCR_SOC	M26
VDDCR_SOC	M29
VDDCR_SOC	M30
VDDCR_SOC	M33
VDDCR_SOC	M34
VDDCR_SOC	M35
VDDCR_SOC	M36
VDDCR_SOC	M39
VDDCR_SOC	M43
VDDCR_SOC	M45
VDDCR_SOC	N13
VDDCR_SOC	N14
VDDCR_SOC	N17
VDDCR_SOC	N18
VDDCR_SOC	N21
VDDCR_SOC	N22
VDDCR_SOC	N25
VDDCR_SOC	N26
VDDCR_SOC	N29
VDDCR_SOC	N30
VDDCR_SOC	N45
VDDCR_SOC	P13
VDDCR_SOC	P14
VDDCR_SOC	P17
VDDCR_SOC	P18
VDDCR_SOC	P21
VDDCR_SOC	P22
VDDCR_SOC	P25
VDDCR_SOC	P26
VDDCR_SOC	P29
VDDCR_SOC	P30
VDDCR_SOC	P45
VDDCR_SOC	R13
VDDCR_SOC	R14
VDDCR_SOC	R17
VDDCR_SOC	R18
VDDCR_SOC	R21
VDDCR_SOC	R22
VDDCR_SOC	R25
VDDCR_SOC	R26
VDDCR_SOC	R29
VDDCR_SOC	R30

Signal Name	Ball Reference
VDDCR_SOC	R31
VDDCR_SOC	R32
VDDCR_SOC	R33
VDDCR_SOC	R34
VDDCR_SOC	R35
VDDCR_SOC	R36
VDDCR_SOC	R37
VDDCR_SOC	R41
VDDCR_SOC	R45
VDDCR_SOC	T13
VDDCR_SOC	T14
VDDCR_SOC	T17
VDDCR_SOC	T18
VDDCR_SOC	T21
VDDCR_SOC	T22
VDDCR_SOC	T25
VDDCR_SOC	T26
VDDCR_SOC	T29
VDDCR_SOC	T30
VDDCR_SOC	T31
VDDCR_SOC	T32
VDDCR_SOC	T33
VDDCR_SOC	T34
VDDCR_SOC	T35
VDDCR_SOC	T36
VDDCR_SOC	T39
VDDCR_SOC	T43
VDDCR_SOC	T45
VDDCR_SOC	U13
VDDCR_SOC	U14
VDDCR_SOC	U17
VDDCR_SOC	U18
VDDCR_SOC	U21
VDDCR_SOC	U22
VDDCR_SOC	U25
VDDCR_SOC	U26
VDDCR_SOC	U45
VDDCR_SOC	V13
VDDCR_SOC	V14
VDDCR_SOC	V17
VDDCR_SOC	V18
VDDCR_SOC	V21

Signal Name	Ball Reference
VDDCR_SOC	V22
VDDCR_SOC	V25
VDDCR_SOC	V26
VDDCR_SOC	V45
VDDCR_SOC	W13
VDDCR_SOC	W14
VDDCR_SOC	W17
VDDCR_SOC	W18
VDDCR_SOC	W21
VDDCR_SOC	W22
VDDCR_SOC	W25
VDDCR_SOC	W26
VDDCR_SOC	W27
VDDCR_SOC	W28
VDDCR_SOC	W29
VDDCR_SOC	W30
VDDCR_SOC	W31
VDDCR_SOC	W32
VDDCR_SOC	W33
VDDCR_SOC	W34
VDDCR_SOC	W35
VDDCR_SOC	W36
VDDCR_SOC	W37
VDDCR_SOC	W41
VDDCR_SOC	W45
VDDCR_SOC	Y13
VDDCR_SOC	Y14
VDDCR_SOC	Y17
VDDCR_SOC	Y18
VDDCR_SOC	Y21
VDDCR_SOC	Y22
VDDCR_SOC	Y25
VDDCR_SOC	Y26
VDDCR_SOC	Y27
VDDCR_SOC	Y28
VDDCR_SOC	Y29
VDDCR_SOC	Y30
VDDCR_SOC	Y31
VDDCR_SOC	Y32
VDDCR_SOC	Y33
VDDCR_SOC	Y34
VDDCR_SOC	Y35

Signal Name	Ball Reference
VDDCR_SOC	Y36
VDDCR_SOC	Y39
VDDCR_SOC	Y43
VDDCR_SOC	Y45
VDDCR_SOC	AA13
VDDCR_SOC	AA14
VDDCR_SOC	AA17
VDDCR_SOC	AA18
VDDCR_SOC	AA21
VDDCR_SOC	AA22
VDDCR_SOC	AA45
VDDCR_SOC	AB13
VDDCR_SOC	AB14
VDDCR_SOC	AB17
VDDCR_SOC	AB18
VDDCR_SOC	AB21
VDDCR_SOC	AB22
VDDCR_SOC	AB45
VDDCR_SOC	AC13
VDDCR_SOC	AC14
VDDCR_SOC	AC17
VDDCR_SOC	AC18
VDDCR_SOC	AC21
VDDCR_SOC	AC22
VDDCR_SOC	AC23
VDDCR_SOC	AC24
VDDCR_SOC	AC25
VDDCR_SOC	AC26
VDDCR_SOC	AC27
VDDCR_SOC	AC28
VDDCR_SOC	AC29
VDDCR_SOC	AC30
VDDCR_SOC	AC31
VDDCR_SOC	AC32
VDDCR_SOC	AC33
VDDCR_SOC	AC34
VDDCR_SOC	AC35
VDDCR_SOC	AC36
VDDCR_SOC	AC37
VDDCR_SOC	AC41
VDDCR_SOC	AC45
VDDCR_SOC	AD13

Signal Name	Ball Reference
VDDCR_SOC	AD14
VDDCR_SOC	AD17
VDDCR_SOC	AD18
VDDCR_SOC	AD21
VDDCR_SOC	AD22
VDDCR_SOC	AD23
VDDCR_SOC	AD24
VDDCR_SOC	AD25
VDDCR_SOC	AD26
VDDCR_SOC	AD27
VDDCR_SOC	AD28
VDDCR_SOC	AD29
VDDCR_SOC	AD30
VDDCR_SOC	AD31
VDDCR_SOC	AD32
VDDCR_SOC	AD33
VDDCR_SOC	AD34
VDDCR_SOC	AD35
VDDCR_SOC	AD36
VDDCR_SOC	AD39
VDDCR_SOC	AD43
VDDCR_SOC	AD45
VDDCR_SOC	AE13
VDDCR_SOC	AE14
VDDCR_SOC	AE17
VDDCR_SOC	AE18
VDDCR_SOC	AE45
VDDCR_SOC	AF17
VDDCR_SOC	AF18
VDDCR_SOC	AF45
VDDCR_SOC	AG17
VDDCR_SOC	AG18
VDDCR_SOC	AG19
VDDCR_SOC	AG20
VDDCR_SOC	AG21
VDDCR_SOC	AG22
VDDCR_SOC	AG23
VDDCR_SOC	AG24
VDDCR_SOC	AG25
VDDCR_SOC	AG26
VDDCR_SOC	AG27
VDDCR_SOC	AG28

Signal Name	Ball Reference
VDDCR_SOC	AG29
VDDCR_SOC	AG30
VDDCR_SOC	AG31
VDDCR_SOC	AG32
VDDCR_SOC	AG33
VDDCR_SOC	AG34
VDDCR_SOC	AG35
VDDCR_SOC	AG36
VDDCR_SOC	AG37
VDDCR_SOC	AG41
VDDCR_SOC	AG45
VDDCR_SOC	AH18
VDDCR_SOC	AH19
VDDCR_SOC	AH20
VDDCR_SOC	AH21
VDDCR_SOC	AH22
VDDCR_SOC	AH23
VDDCR_SOC	AH24
VDDCR_SOC	AH25
VDDCR_SOC	AH26
VDDCR_SOC	AH27
VDDCR_SOC	AH28
VDDCR_SOC	AH29
VDDCR_SOC	AH30
VDDCR_SOC	AH31
VDDCR_SOC	AH32
VDDCR_SOC	AH33
VDDCR_SOC	AH34
VDDCR_SOC	AH35
VDDCR_SOC	AH36
VDDCR_SOC	AH39
VDDCR_SOC	AH43
VDDCR_SOC	AH45
VDDCR_SOC	AJ45
VDDCR_SOC	AK45
VDDCR_SOC	AL41
VDDCR_SOC	AL45
VDDCR_SOC	AM39
VDDCR_SOC	AM43
VDDCR_SOC	AM44
VDDCR_SOC	AM45
VDDCR_SOC	AN43

Signal Name	Ball Reference
VDDCR_SOC	AN44
VDDCR_SOC	AN45
VDDCR_SOC	AP42
VDDCR_SOC	AP43
VDDCR_SOC	AP44
VDDCR_SOC	AP45
VDDCR_SOC	AR41
VDDCR_SOC	AR42
VDDCR_SOC	AR43
VDDCR_SOC	AR44
VDDCR_SOC	AT39
VDDCR_SOC	AT40
VDDCR_SOC	AT41
VDDCR_SOC	AT42
VDDCR_SOC	AU38
VDDCR_SOC	AU39
VDDCR_SOC	AU40
VDDCR_SOC	AU41
VDDIO_MEM	AP16
VDDIO_MEM	AP30
VDDIO_MEM	AR19
VDDIO_MEM	AR22
VDDIO_MEM	AR25
VDDIO_MEM	AR28
VDDIO_MEM	AR31
VDDIO_MEM	AT17
VDDIO_MEM	AT18
VDDIO_MEM	AT21
VDDIO_MEM	AT24
VDDIO_MEM	AT27
VDDIO_MEM	AT30
VDDIO_MEM	AT33
VDDIO_MEM	AU19
VDDIO_MEM	AU24
VDDIO_MEM	AV24
VDDIO_MEM	AV26
VDDIO_MEM	AV27
VDDIO_MEM	AW30
VDDIO_MEM	AW33
VDDIO_MEM	AW36
VDDIO_MEM	AY24
VDDIO_MEM	AY32

Signal Name	Ball Reference
VDDIO_MEM	AY35
VDDIO_MEM	AY38
VDDIO_MEM	BB33
VDDIO_MEM	BB35
VDDIO_MEM	BB36
VDDIO_MEM	BB39
VDD_18	Y5
VDD_18	Y6
VDD_18	AA5
VDD_18	AB5
VDD_18	AB6
VDD_18	AC6
VDD_18	AE6
VDD_18	AG4
VDD_18	AG5
VDD_18	AH5
VDD_080	AL7
VDD_080	AM8
VDD_080	AP8
VDD_080	AT8
VDD_080	AV4
VDD_080	AV7
VDD_080	AV10
VDD_080	AW3
VDD_080	AW6
VDD_080	AW9
VDD_080_EFUSE	AK8
VDD_080_EFUSE	AK9
VPP	BD26
VPP	BE26
VPP	BE27
VREFEXTA	AR15
VREFEXTB	AR36
VSS	B3
VSS	B7
VSS	B11
VSS	B39
VSS	B43
VSS	C5
VSS	C9
VSS	C13
VSS	C17

Signal Name	Ball Reference
VSS	C21
VSS	C25
VSS	C29
VSS	C33
VSS	C37
VSS	C41
VSS	D1
VSS	D7
VSS	D11
VSS	D39
VSS	D43
VSS	E2
VSS	E5
VSS	E9
VSS	E13
VSS	E17
VSS	E21
VSS	E25
VSS	E29
VSS	E33
VSS	E37
VSS	E41
VSS	F1
VSS	F4
VSS	F7
VSS	F11
VSS	F39
VSS	F43
VSS	G3
VSS	G6
VSS	G9
VSS	G13
VSS	G17
VSS	G21
VSS	G25
VSS	G29
VSS	G33
VSS	G37
VSS	G41
VSS	H1
VSS	H4
VSS	H7

Signal Name	Ball Reference
VSS	H11
VSS	J3
VSS	J6
VSS	J9
VSS	J37
VSS	J41
VSS	K1
VSS	K4
VSS	K7
VSS	K11
VSS	K12
VSS	K15
VSS	K16
VSS	K19
VSS	K20
VSS	K23
VSS	K24
VSS	K27
VSS	K28
VSS	K31
VSS	K32
VSS	K35
VSS	K36
VSS	L3
VSS	L5
VSS	L9
VSS	L12
VSS	L15
VSS	L16
VSS	L19
VSS	L20
VSS	L23
VSS	L24
VSS	L27
VSS	L28
VSS	L31
VSS	L32
VSS	M1
VSS	M4
VSS	M7
VSS	M11
VSS	M12

Signal Name	Ball Reference
VSS	M15
VSS	M16
VSS	M19
VSS	M20
VSS	M23
VSS	M24
VSS	M27
VSS	M28
VSS	M31
VSS	M32
VSS	N3
VSS	N5
VSS	N9
VSS	N12
VSS	N15
VSS	N16
VSS	N19
VSS	N20
VSS	N23
VSS	N24
VSS	N27
VSS	N28
VSS	N31
VSS	N32
VSS	N33
VSS	N34
VSS	N35
VSS	N36
VSS	N37
VSS	N41
VSS	P1
VSS	P4
VSS	P7
VSS	P11
VSS	P12
VSS	P15
VSS	P16
VSS	P19
VSS	P20
VSS	P23
VSS	P24
VSS	P27

Signal Name	Ball Reference
VSS	P28
VSS	P31
VSS	P32
VSS	P33
VSS	P34
VSS	P35
VSS	P36
VSS	P39
VSS	P43
VSS	R3
VSS	R6
VSS	R9
VSS	R12
VSS	R15
VSS	R16
VSS	R19
VSS	R20
VSS	R23
VSS	R24
VSS	R27
VSS	R28
VSS	T1
VSS	T4
VSS	T7
VSS	T11
VSS	T12
VSS	T15
VSS	T16
VSS	T19
VSS	T20
VSS	T23
VSS	T24
VSS	T27
VSS	T28
VSS	U3
VSS	U6
VSS	U9
VSS	U12
VSS	U15
VSS	U16
VSS	U19
VSS	U20

Signal Name	Ball Reference
VSS	U23
VSS	U24
VSS	U27
VSS	U28
VSS	U29
VSS	U30
VSS	U31
VSS	U32
VSS	U33
VSS	U34
VSS	U35
VSS	U36
VSS	U37
VSS	U41
VSS	V1
VSS	V4
VSS	V8
VSS	V11
VSS	V12
VSS	V15
VSS	V16
VSS	V19
VSS	V20
VSS	V23
VSS	V24
VSS	V27
VSS	V28
VSS	V29
VSS	V30
VSS	V31
VSS	V32
VSS	V33
VSS	V34
VSS	V35
VSS	V36
VSS	V39
VSS	V43
VSS	W3
VSS	W6
VSS	W9
VSS	W12
VSS	W15

Signal Name	Ball Reference
VSS	W16
VSS	W19
VSS	W20
VSS	W23
VSS	W24
VSS	Y1
VSS	Y4
VSS	Y8
VSS	Y11
VSS	Y12
VSS	Y15
VSS	Y16
VSS	Y19
VSS	Y20
VSS	Y23
VSS	Y24
VSS	AA3
VSS	AA6
VSS	AA9
VSS	AA12
VSS	AA15
VSS	AA16
VSS	AA19
VSS	AA20
VSS	AA23
VSS	AA24
VSS	AA25
VSS	AA26
VSS	AA27
VSS	AA28
VSS	AA29
VSS	AA30
VSS	AA31
VSS	AA32
VSS	AA33
VSS	AA34
VSS	AA35
VSS	AA36
VSS	AA37
VSS	AA41
VSS	AB1
VSS	AB4

Signal Name	Ball Reference
VSS	AB7
VSS	AB11
VSS	AB12
VSS	AB15
VSS	AB16
VSS	AB19
VSS	AB20
VSS	AB23
VSS	AB24
VSS	AB25
VSS	AB26
VSS	AB27
VSS	AB28
VSS	AB29
VSS	AB30
VSS	AB31
VSS	AB32
VSS	AB33
VSS	AB34
VSS	AB35
VSS	AB36
VSS	AB39
VSS	AB43
VSS	AC3
VSS	AC5
VSS	AC9
VSS	AC12
VSS	AC15
VSS	AC16
VSS	AC19
VSS	AC20
VSS	AD1
VSS	AD4
VSS	AD7
VSS	AD11
VSS	AD12
VSS	AD15
VSS	AD16
VSS	AD19
VSS	AD20
VSS	AE3
VSS	AE5

Signal Name	Ball Reference
VSS	AE9
VSS	AE12
VSS	AE15
VSS	AE16
VSS	AE19
VSS	AE20
VSS	AE21
VSS	AE22
VSS	AE23
VSS	AE24
VSS	AE25
VSS	AE26
VSS	AE27
VSS	AE28
VSS	AE29
VSS	AE30
VSS	AE31
VSS	AE32
VSS	AE33
VSS	AE34
VSS	AE35
VSS	AE36
VSS	AE37
VSS	AE41
VSS	AF1
VSS	AF4
VSS	AF7
VSS	AF11
VSS	AF12
VSS	AF13
VSS	AF14
VSS	AF15
VSS	AF16
VSS	AF19
VSS	AF20
VSS	AF21
VSS	AF22
VSS	AF23
VSS	AF24
VSS	AF25
VSS	AF26
VSS	AF27

Signal Name	Ball Reference
VSS	AF28
VSS	AF29
VSS	AF30
VSS	AF31
VSS	AF32
VSS	AF33
VSS	AF34
VSS	AF35
VSS	AF36
VSS	AF39
VSS	AF43
VSS	AG3
VSS	AG12
VSS	AG13
VSS	AG14
VSS	AG15
VSS	AG16
VSS	AH1
VSS	AH4
VSS	AH7
VSS	AH8
VSS	AH11
VSS	AH12
VSS	AH13
VSS	AH14
VSS	AH15
VSS	AH16
VSS	AJ3
VSS	AJ6
VSS	AJ9
VSS	AJ12
VSS	AJ13
VSS	AJ19
VSS	AJ22
VSS	AJ25
VSS	AJ28
VSS	AJ31
VSS	AJ34
VSS	AJ37
VSS	AJ41
VSS	AK1
VSS	AK4

Signal Name	Ball Reference
VSS	AK6
VSS	AK11
VSS	AK12
VSS	AK13
VSS	AK18
VSS	AK21
VSS	AK24
VSS	AK27
VSS	AK30
VSS	AK33
VSS	AK36
VSS	AK37
VSS	AK39
VSS	AK43
VSS	AL1
VSS	AL3
VSS	AL9
VSS	AL12
VSS	AL13
VSS	AL16
VSS	AM2
VSS	AM4
VSS	AM7
VSS	AM11
VSS	AM12
VSS	AM13
VSS	AM16
VSS	AN7
VSS	AN9
VSS	AN13
VSS	AN16
VSS	AN18
VSS	AN21
VSS	AN24
VSS	AN27
VSS	AN30
VSS	AN33
VSS	AN36
VSS	AN41
VSS	AP7
VSS	AP11
VSS	AP12

Signal Name	Ball Reference
VSS	AP13
VSS	AP17
VSS	AP20
VSS	AP23
VSS	AP26
VSS	AP29
VSS	AP32
VSS	AP35
VSS	AR3
VSS	AR7
VSS	AR9
VSS	AR12
VSS	AR13
VSS	AR16
VSS	AT3
VSS	AT7
VSS	AT11
VSS	AT13
VSS	AT15
VSS	AT38
VSS	AU10
VSS	AU12
VSS	AU13
VSS	AU17
VSS	AU20
VSS	AU23
VSS	AU26
VSS	AU29
VSS	AU32
VSS	AU35
VSS	AU45
VSS	AV5
VSS	AV6
VSS	AV9
VSS	AV11
VSS	AV25
VSS	AV28
VSS	AV31
VSS	AV34
VSS	AV37
VSS	AV43
VSS	AW4

Signal Name	Ball Reference
VSS	AW5
VSS	AW8
VSS	AW11
VSS	AW14
VSS	AW17
VSS	AW18
VSS	AW19
VSS	AW20
VSS	AW21
VSS	AW22
VSS	AW41
VSS	AW45
VSS	AY4
VSS	AY7
VSS	AY10
VSS	AY13
VSS	AY16
VSS	AY19
VSS	AY22
VSS	AY39
VSS	AY43
VSS	BA5
VSS	BA6
VSS	BA9
VSS	BA12
VSS	BA15
VSS	BA18
VSS	BA21
VSS	BA22
VSS	BA27
VSS	BA31
VSS	BA34
VSS	BA37
VSS	BA41
VSS	BB4
VSS	BB5
VSS	BB8
VSS	BB11
VSS	BB14
VSS	BB17
VSS	BB20
VSS	BB23

Signal Name	Ball Reference
VSS	BB28
VSS	BB29
VSS	BB30
VSS	BB42
VSS	BB44
VSS	BB45
VSS	BC4
VSS	BC7
VSS	BC10
VSS	BC13
VSS	BC16
VSS	BC19
VSS	BC22
VSS	BC25
VSS	BC30
VSS	BC32
VSS	BC35
VSS	BC38
VSS	BC41
VSS	BC44
VSS	BC45
VSS	BD1
VSS	BD5
VSS	BD6
VSS	BD9
VSS	BD12
VSS	BD15
VSS	BD18
VSS	BD21
VSS	BD23
VSS	BD25
VSS	BD34
VSS	BD37
VSS	BD40
VSS	BD43
VSS	BD44
VSS	BD45
VSS	BE2
VSS	BE4
VSS	BE8
VSS	BE11
VSS	BE14

Signal Name	Ball Reference
VSS	BE17
VSS	BE20
VSS	BE21
VSS	BE25
VSS	BE28
VSS	BE34
VSS	BE37
VSS	BE39
VSS	BE42
VSS	BE43
VSS	BE44
WAKEB	BD2
XTALIN	AM1
XTALOUT	AM3
XTRIG6	AD9
XTRIG7	AG9